VHDL Based Simulation of a Delta-Sigma A/D Converter Clocked with a Phased-Locked Loop

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Abstract

The VHDL based mixed-signal event-driven (MixED) simulation method is employed to simulate a comprehensive system containing a number of mixed-signal building blocks: an analog waveform generator, a phase-locked loop and two ΔΣ modulators for A/D conversion.

1 Introduction

Although the range of possible applications of the VHDL based MixED module [1] is smaller than the respective range of other mixed-signal simulators, e.g. [2-4], the MixED system has been shown to allow for a number of useful mixed-signal simulations, e.g. an analog inverter with operational amplifier (OA) [5], a switched capacitor circuit with OA [6], a phase-locked loop (PLL) [7] and a ΔΣ modulator [8]. The latter was verified using PSpice simulations and measured data [9,10].

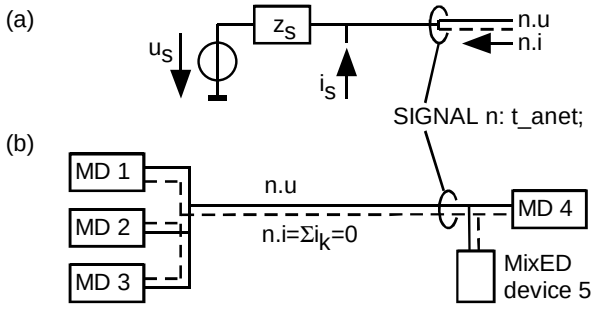

Figure 1.1: (a) MixED analog port driver, **(b)** MixED analog port driver compute the node voltage **n.u** such, that the current sum **n.i** of the net becomes zero.

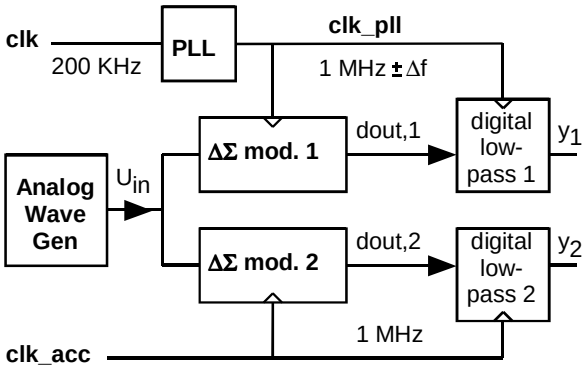

Figure 1.2: Simulated mixed-signal system: analog waveform generator, PLL, two ΔΣ modulators, filters.

A VHDL data type (t_anet) is defined to model an "analog net". It contains resolved real fields that sum connected drivers of type REAL. Such a pseudo-analog port contributes a source voltage u_s, an output impedance z_s and source current i_s to the pseudo-analog net as shown in Fig.1.1(a). An arbitrary number of MixED drivers may drive a signal interpreted as "analog net". MixED drivers connected to form an analog net seek to adjust the node voltage (n.u in Fig. 1.1) such that the current sum (n.i in Fig. 1.1) becomes zero according to Kirchhoff's current law. The models for u_s, z_s and i_s are supplied as subprograms. Moderate non-linearities are allowed (e.g. a CMOS inverter) but cause iterations. Every analog net performs its own, adaptive time stepping. MixED drivers are suitable for modeling uni-directional devices such as digital gates, DACs, ADCs, VCOs, PLLs, buffered analog multiplexers and demultiplexers, etc.

Fig. 1.2 illustrates the system under investigation in this communication. The contained mixed-signal circuits are a waveform generator, a PLL and two ΔΣ modulators. One of the modulators is clocked by the PLL, the other receives an ideal clock signal.

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2 The Phase-Locked Loop (PLL)

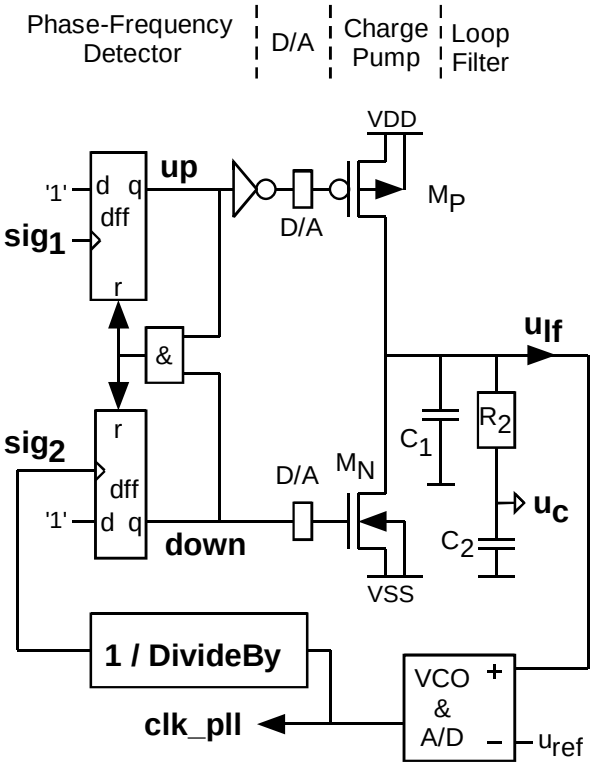

Figure 2.1: Schematics of the phase-locked loop.

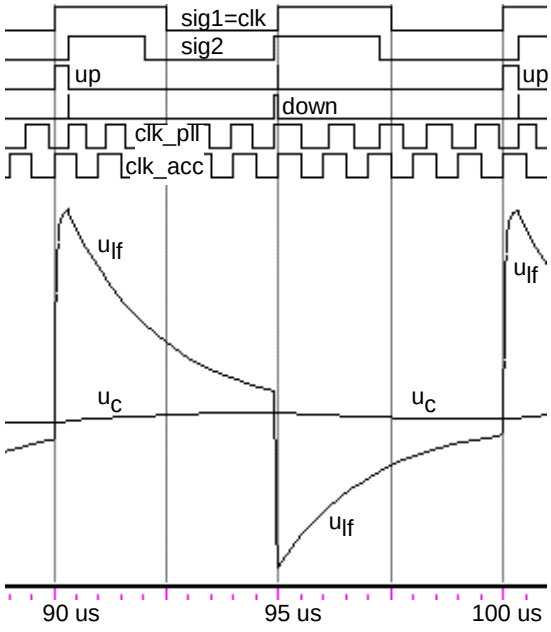

Figure 2.2: Signals of the PLL shown in Fig. 2.1.

A VHDL based MixED simulation of the phase-locked loop (PLL) shown Fig. 2.1 was presented in [7]. This PLL is also termed digital PLL (DPLL) as it has digital external ports only. The signal sig_1 in Fig. 2.1 is connected to the external signal clk in Fig. 1.2. The feedback loop seeks to synchronize the rising edges of sig_1 and sig_2. The width of the signals named 'up' and 'down' in Fig. 2.1 corresponds to the phase error as can be seen from Figs. 2.2 and 2.3.

The signals 'up' and 'down' open the charge pump MOSFETs MP and MN, respectively. Consequently, the loop filter voltage ulf on C_1 rises against V_{DD}=5V or V_{SS}=0V. Most PLL models use ideal current sources instead of FETs and thus risk to simulate voltages ulf>V_{DD} and ulf<V_{SS} [11]. When both FETs are highly impedant, C_1=336pF discharges through R_2=6.5KΩ. Then ulf approaches uc, the voltage across C_2=6.72nF. As the frequency divider divides by 5 in this case, the average frequency of clk_pll must be $5 \cdot f_{clk}$. Signal sig_2 remains high for two cycles of clk_pll and low for 3 cycles. Due to this asymmetry only rising edges may be compared.

Comparing the rising edges of clk_pll and sig_2 in Fig. 2.2 with the rising edge of the reference clk=sig_1, it is evident that clk_pll and sig_2 have the same absolute phase error. As clk_pll oscillates 5 times faster than sig_2, the relative phase error of clk_pll is 5 times larger than that of sig_2. This results in phase errors up to ±180° of clk_pll with respect to the precise clk_acc. Observing uc in Fig. 2.3 suggests that the phase error of clk_pll contains a periodicity.

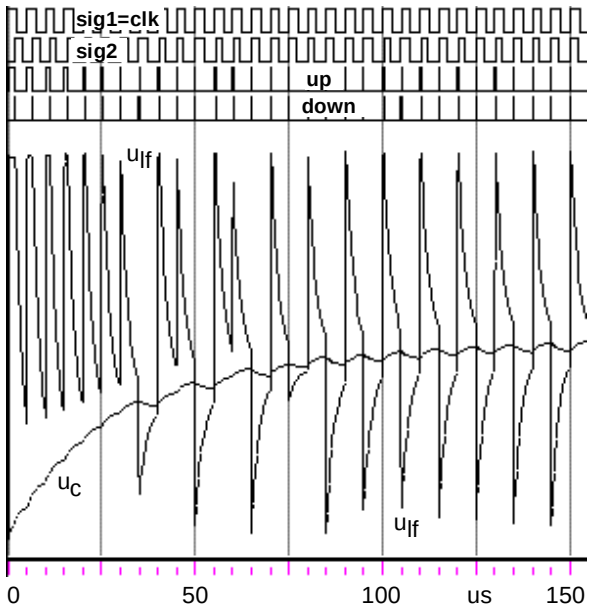

Figure 2.3: Study of PLL internal signals uc and ulf.

3 The ΔΣ modulator as A/D converter

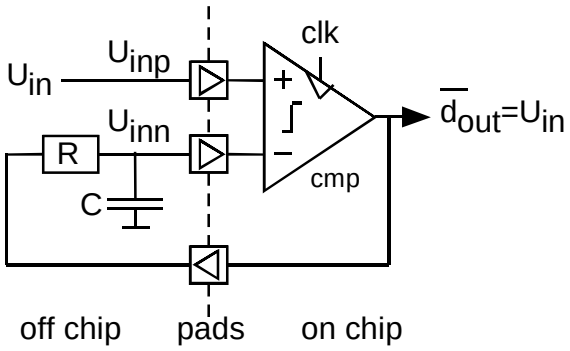

Figure 3.1: ΔΣ-modulator using RC-lowpass as integrator acc. to [8] and [10]: The mean value of d_{out}, termed $d_{out,mean}$, is proportional to U_{in}.

Fig. 3.1 shows a ΔΣ modulator with RC integrator as offered by the institute for Microelectronics Stuttgart [9]. Experimental data for this circuit is contained in [10].

Fig. 3.2 shows a simulation of the circuit shown in Fig. 3.1 obtained with the MixED module running on the ModelSim 5.3 simulator [12]. Results were compared to PSpice-A/D simulations and to measured data taken from [10]. PSpice delivered a transient simulation which was close to that shown in Fig. 3.2 [8]. Experimental statistical data was close to simulated statistical data [8].

Some major problems of this 1st order modulator for constant input voltage U_{in} can be observed in Fig. 3.2:

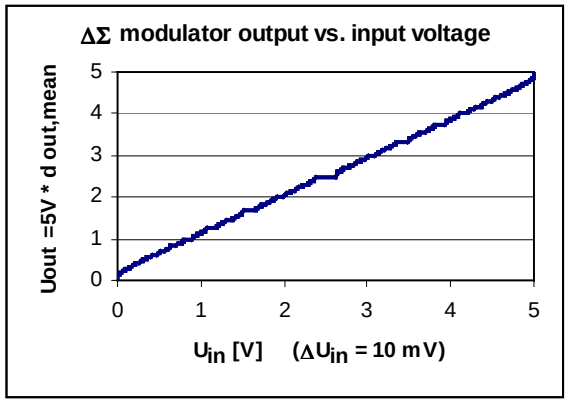

Figure 3.3: Characteristics of the ΔΣ modulator shown in Fig. 3.1 with R=1KΩ, C=1μF.

(1) Pattern noise: For DC input the modulator tends to repeat bit sequences of m bits corresponding to a frequency of f_{clk}/m, which can become low.
(2) Dead zone noise: The same sequence of decisions taken in Fig. 3.2 for constant U_{in} would also be taken for some $U_{in}\pm\Delta u$. This problem is severe for low gain integrators.
(3) Leakage in the integrator: The RC integrator employed is non-ideal and increases noise specifically at frequencies lower than $\omega_g=1/RC$.

Problems (1) and (2) can be alleviated by high loop gain, by adding a high frequency dither noise [14] to the input signal or by introducing clock jitter as demonstrated by the PLL to disturb the regularity of the bit patterns. Another possibility is the use of higher order modulators.

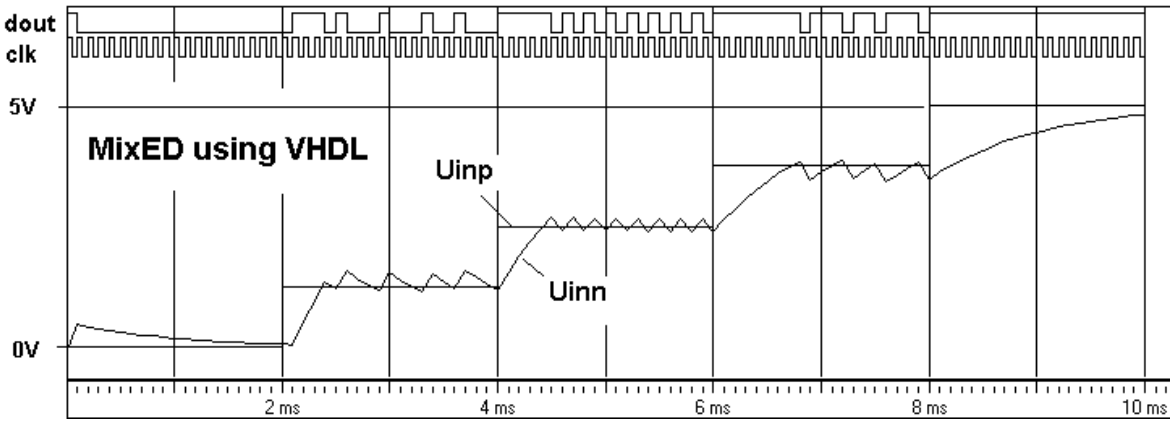

Figure 3.2: Screen shot of a simulation of the ΔΣ modulator shown in Fig. 3.1. The density of bits on d_{out} is proportional to $u_{inp}=u_{in}$, that steps from 0...5V with a step size of 1.25V. Parameters: R=1KΩ, C=1μF and f_{clk}=10KHz. The simulation was performed with the VHDL-based MixED module on ModelSim 5.3 [12].

4 Using the PLL to clock the ΔΣ modulator

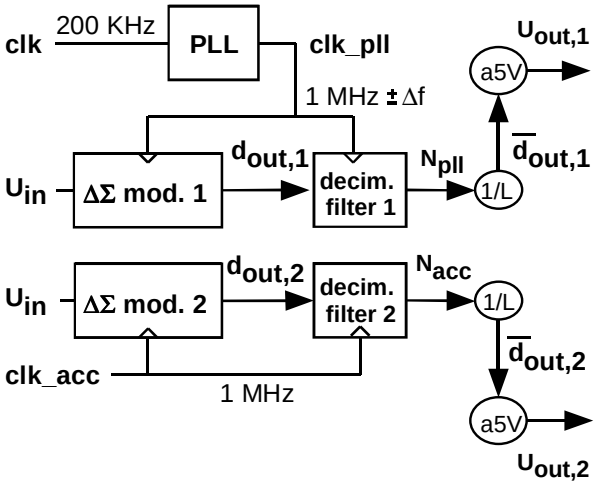

Figure 4.1: Simulated mixed-signal structure.

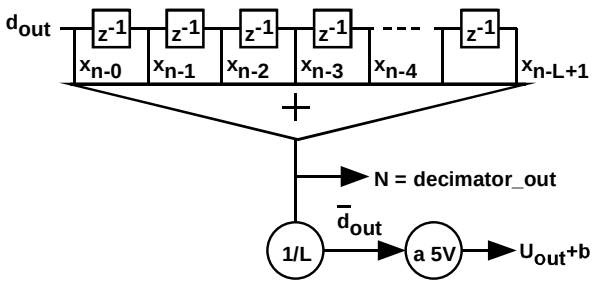

Figure 4.2: Employed decimation filter and scaling.

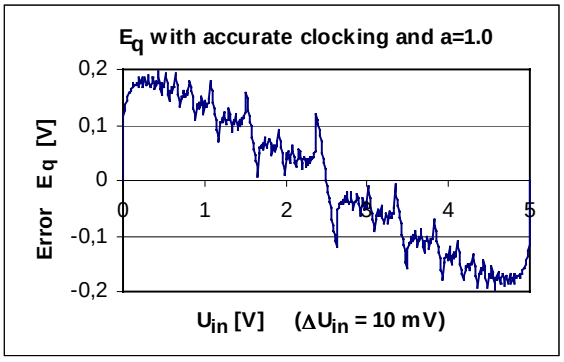

Figure 4.3: A/D conversion error E_q versus input voltage U_{in} of accurately clocked ΔΣ modulator using a=1.0 and b=0 in Eq. (2).

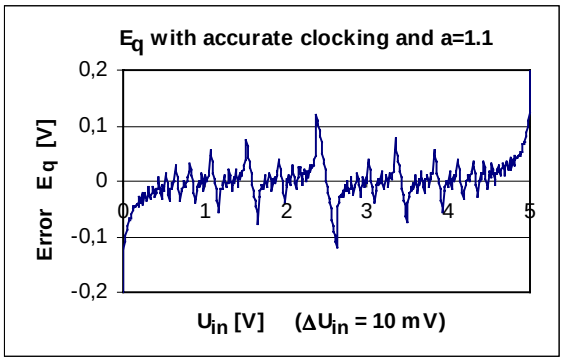

Figure 4.4: A/D conversion error E_q versus input voltage of accurately clocked modulator, a=1.1.

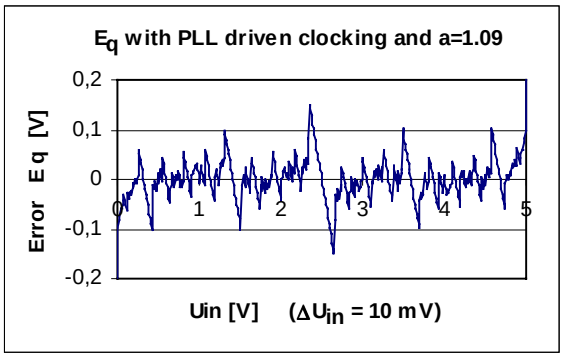

Figure 4.5: A/D conversion error E_q versus input voltage U_{in} of ΔΣ modulator clocked with the PLL's output signal clk_pll; a=1.09, b=-0.225 in Eq. (2).

Fig. 4.1 illustrates the simulated mixed-signal structure: The ΔΣ modulators 1 and 2 receive the same input voltage U_{in}. Modulator 1 and decimator 1 are clocked with the noisy clock signal clk_pll having a frequency of 1 MHz ± Δf; with Δf modeling the noise of the PLL. Modulator 2 and decimator 2 are clocked with the accurate clock signal clk_acc having a frequency of exactly 1MHz.

Fig. 4.2 illustrates further details of the decimation and signal conditioning process: the output of the decimator, N, is the number of '1'-states contained in the last L input bits. For this report L=500 was employed. The mean value of dout was computed after N became stable from

$$dout\_mean = N / L \qquad (1)$$

Eq. (1) delivers a mean value in the range of $0 \le dout\_mean \le 1$. To obtain an output voltage that

should ideally equal the input voltage, one more transformation is necessary:

$$Uout = a\,(V_{DD}\text{-}V_{SS})\ dout\_mean + b. \qquad (2)$$

Fig. 4.6 illustrates the accruement of pattern noise and dead zone noise. For constant input voltage, certain voltage levels can be represented by rational numbers m/n, which is 3/5 in Fig. 4.6. The modulator's output repeats a pattern sequence of 5 bits. Long bit sequences causing low frequency noise may appear as pattern noise. Moving the input voltage within the dead zone, i.e. without crossing one of the clocked comparator's decision points, has no impact on the output bit stream. Therefore, the computed output voltage remains constant and causes the error peaks shown in Figs. 4.3 – 4.5. HF dither noise injection can alleviate the dead zone problem [14]. Surprisingly, the noisy clock signal does not alleviate this phenomenon in all situations which may be due to the fact that the simulated phase noise of clk_pll is not sufficiently white.

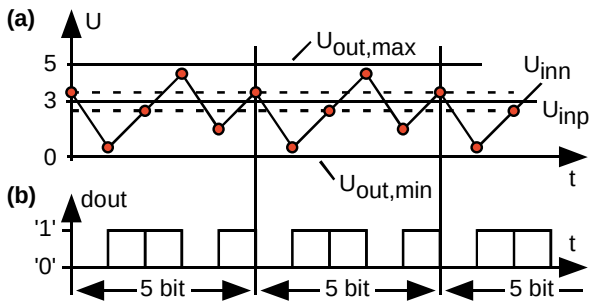

Figure 4.6: Pattern noise and dead zone: a bit pattern of five bits is continuously repeated for a range of U_{inp}.

5 Conclusions

The VHDL based MixED module is shown to be capable of simulating a mixed-signal system containing the following mixed-signal devices: (1) An analog waveform generator, (2) a phase-locked loop and (3) two ΔΣ modulators with RC integrator operating as A/D converters. One ΔΣ modulator receives its clock signal from the output of the PLL, the other receives a precise 1 MHz clock signal. The MixED simulation of this system permits the investigation of a number of related questions.

The simulation speed with the not yet speed optimized MixED module equals approximately 37 simulated clock cycles per second CPU time on a 733 MHz Intel Pentium III processor operated under Microsoft Windows NT 4.0.

6 Acknowledgments

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7 References

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