Operational Amplifier Modeling Using Event-Driven VHDL

Martin Schubert

Fachhochschule[1)] Regensburg, D-93053 Regensburg, Seybothstr. 2
e-mail: martin.schubert@e-technik.fh-regensburg.de
Phone +49 / 941 / 943-1104, FAX: -1424

[1)] Application-oriented university providing degree-courses particularly in engineering, economics, social work and design.

Abstract

A method to model high-gain feedback-loop analog amplifiers on an event driven time axis is presented. The demonstrator is coded in digital VHDL'93. In the event-driven scheme any node in the network must converge „on its own" based on the information delivered from its neighbors, as no overall matrix is set up. For this reason signal loops with a loop gain larger than one are typically unstable. This communication presents a numerically stable generic model for high gain amplifiers with a user defined feedback network. Non-ideal effects like offset or finite gain can be taken into account.

1 Introduction

1.1 Concurrent Event-Driven Analog Modeling: State of the Art

A method to perform mixed analog-digital signal modeling on an event driven time axis was presented [1-3]. The proposed iteration scheme is not limited to a specific hardware description language (HDL), but can be coded on any event-driven simulator that offers some basic preconditions: (1) real-number processing, (2) zero-delay time stepping and (3) user definable resolution functions. In the case presented here, the MixED (Mixed signal Event Driven) Simulator was developed and coded in VHDL to demonstrate the method. Generic models for linear components and controlled sources were proposed, allowing for implicit backward Euler integration of the differential equations.

Controlled linear sources and passive linear devices such as generic models for resistors, capacitors and inductors were presented [1-3]. This communication shows this method is applicable to some active devices like high loop gain operational amplifiers (OpAmps). A generic amplifier model is presented allowing for user defined feedback networks.

1.2 Available Components

According to [3] three source types are available as illustrated in Fig. 1.1 (a-c): They are single-ended, combined voltage and current sources.

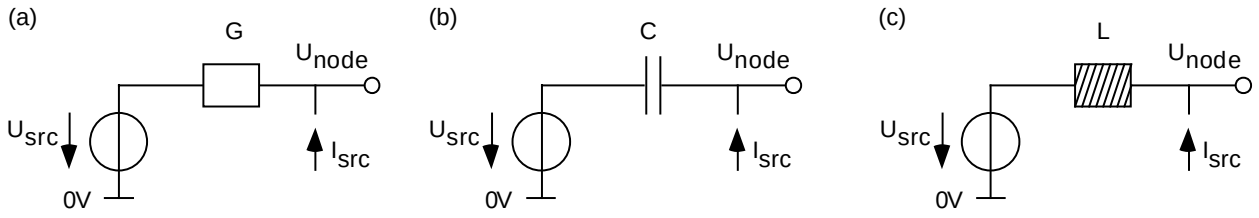


Figure 1.1:
Single-ended voltage and current sources: **(a)** resistive, **(b)** capacitive, **(c)** inductive.

To illustrate some possibilities of circuit modeling using these source types Fig. 1.2 shows the resistive source type of Fig. 1.1(a) employed to simulate a current mirror used as a current source. The circuit of Fig. 1.2(a) is converted into its small signal equivalent shown in Fig. 1.2(b), which can be simulated using the single-ended resistive source of Fig. 1.1(a) as illustrated in Fig. 1.2(c).

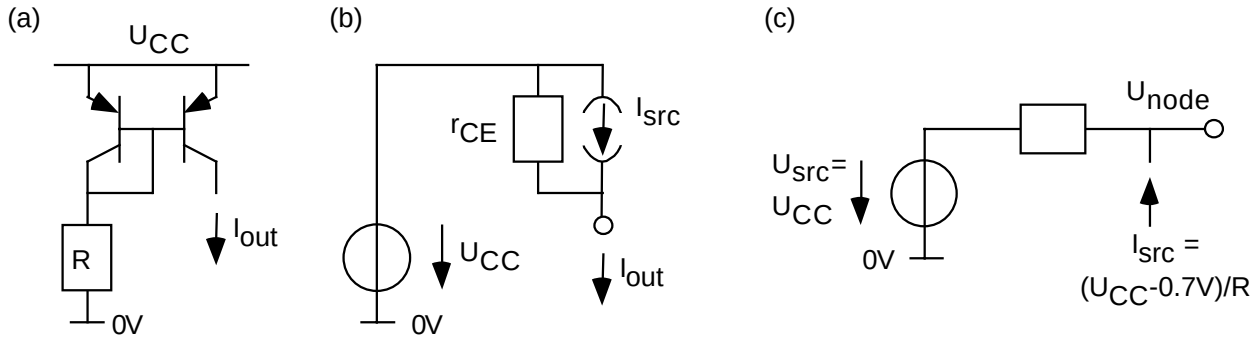


Figure 1.2: Modeling small portions of linear circuitry using the given components:
(a) current mirror, **(b)** small signal model and **(c)** equivalent resistive source according to Fig. 1.1(a)

So far one-terminal devices have been presented. To obtain a generic model for the two-terminal resistor, two of these single-ended, resistive sources can be connected according to Fig. 1.3(a). In the same way two-terminal capacitors and inductors can be obtained. This is easily demonstrated by applying the equations for implicit backward Euler integration.

$$I_C = \frac{dU_C}{dt} \cong C\frac{\Delta U_C}{\Delta t} = \frac{C}{\Delta t}(U_C^{(n+1)} - U_C^{(n)}) \quad (1)$$

$$U_L = L\frac{dI_L}{dt} \cong L\frac{\Delta I_L}{\Delta t} = \frac{L}{\Delta t}(I_L^{(n+1)} - I_L^{(n)}) \quad (2)$$

where $\Delta t = t_{n+1} - t_n$ (3)

As can be seen from these equations the capacitor can be modeled as a conductor $G_C = C/\Delta t$ in series with a voltage source $U^* = U_C^{(n)}$ and the inductor as a resistor $R_L = L/\Delta t$ parallel to a current source $I^* = I_L^{(n)}$, where the sources U* and I* are the respective device quantities at the beginning of the actual time step Δt. Consequently, they are constants during the calculation of the next point in time, i.e. t_{n+1}. On this basis the two-terminal devices resistor, capacitor and inductor can be modeled as illustrated in Fig. 1.3.

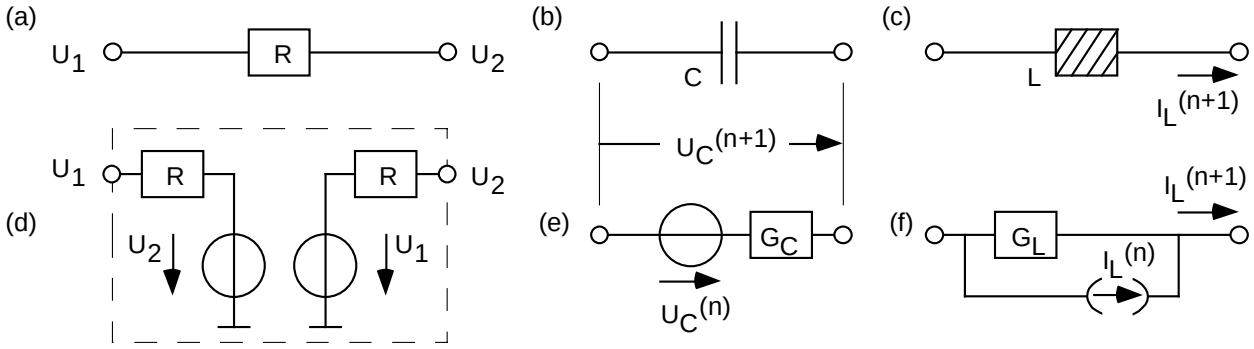


Figure 1.3: Modeling the linear two-terminal devices **(a)** resistor, **(b)** capacitor and **(c)** inductor using the given one-terminal sources: **(d)** The resistor is composed of two resistive sources, **(e)** the capacitor is modeled by a conductor and a voltage source in series, and **(f)** the inductor's behavior is simulated by a resistor and a parallel current source.

The presented components are suitable for the simulation of small portions of circuitry in a large digital design, e.g. the RLC system of an input pad with protection diodes [3]. However, the availability of active devices, specifically operational amplifiers, will significantly increase the scope of applications. Some applications using OpAmps will be presented at the same conference [4].

The need for mixed-signal simulation using operation amplifiers can be seen from a large number of references in this field, e.g. [5-9].

2 A Generic Model for the Operational Amplifier

High gain feedback loops exhibit unstable behavior during concurrent iteration. To obtain a stable behavioral model the feedback-loop is replaced by a feed-forward circuit. The transformation is most simple for an ideal OpAmp (Fig. 2.1). Due to the Miller effect [10] the input resistance of the structure is given by $Z_{in}=Z/(1+A_V)$ with A_V being the OpAmp's amplification. In the assumed ideal case of $A_V \rightarrow \infty$ we have $Z_{in}=0$. The behavior of the models shown in Fig. 2.1(a) and (b) are identical in this case.

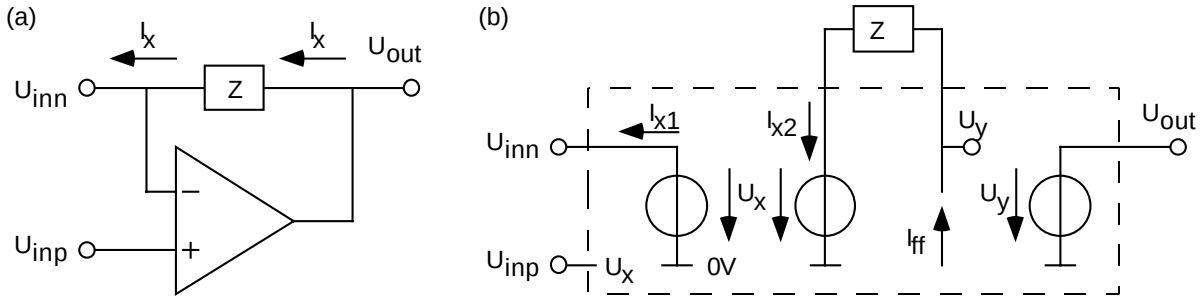


Figure 2.1: **(a)** ideal OpAmp with feedback loop, **(b)** equivalent behavioral model

The ideal OpAmp (A_V, Z_{inn}, Z_{inp} ->∞, $U_{offset}=Z_{out}=0$) forces its negative input to the same voltage as its positive input. This is modeled in Fig. 2.1(b) by two voltage sources $U_x=U_{inp}$. The current I_{x1} into the negative input is measured and the feed-forward current I_{ff} is adjusted such that $I_{x2}=I_{x1}$. Now the situation of the feedback network is identical for both models. In the behavioral feed-forward model the output terminal must be separated from the feedback loop by an additional voltage source $U_y=U_{out}$.

A more general approach using the same strategy is shown in Fig. 2.2. We set e.g.:

$$Z_{in} = Z_{out} = 0, \tag{2.1}$$

$$U_{x1} = U_{ff} = U_{inp} + U_{offset} + U_{out} / A_V, \tag{2.2}$$

$$I_{ff} = I_x. \tag{2.3}$$

The quantities U_{ff} and I_{ff} control the "feedback" network in forward operation, such that $I_{x1}=I_{x2}$ respecting a non-zero offset voltage U_{offset}. A bipolar DC input current I_{in_bip} is also included. According to Miller's law the input impedance of the structure depends on the feedback network which is unknown when coding the behavioral OpAmp model. So the input impedance is better modeled by $U_{x1} \propto U_{out}/A_V$ and $Z_{in}=0$ rather than using constant U_{x1} and a non-zero Z_{in}. Modeling Z_{in} or U_{x1} as f(A_V) causes a new feedback mechanism.

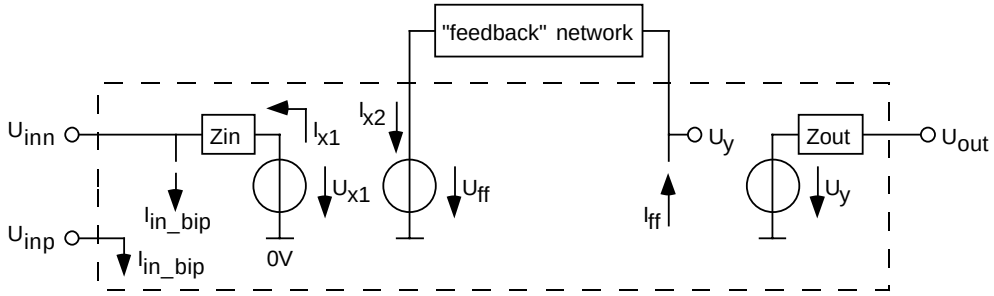


Figure 2.2: Behavioral OpAmp model allowing for offset and finite amplification.

Fig. 2.3 serves for stability investigations. For the following investigations let $k=Z_1/(Z_1+Z_2)$. U_1 and U_{inp} are assumed to be constant while the output voltage has just performed a numerical iteration step $\Delta U_{out}^{(d)}$, where d is the iteration counter.

Case (a): OpAmp operated in the feedback mode: A step $\Delta U_{inn}^{(d)} = k \cdot \Delta U_{out}^{(d)}$ is caused. This forces the output to step by $\Delta U_{out}^{(d)} = -A_V \cdot \Delta U_{inn}^{(d)}$, i.e. by $\boxed{\Delta U_{out}^{(d+1)} = -\Delta U_{out}^{(d)} \cdot kA_V}$.

Case (b): OpAmp operated in the feed-forward mode: A step $\Delta U_{inn}^{(d)} = -\Delta U_{out}^{(d)} / A_V$ is caused which modifies the input current: $\Delta I_{x1}^{(d)} = \Delta U_{inn}^{(d)} / Z_1$. As $I_{ff}^{(d)} = I_{x1}^{(d)}$. We obtain $\Delta U_{out}^{(d+1)} = \Delta U_{inn}^{(d)} + Z_2 \Delta I_{x1}^{(d)}$. Combining these equations delivers $\boxed{\Delta U_{out}^{(d+1)} = -\Delta U_{out}^{(d)} / kA_V}$.

Assuming stability for $\left|\Delta U_{out}^{(d+1)}\right| < \left|\Delta U_{out}^{(d)}\right|$ requires $\left|kA_V\right| < 1$ in the feedback model case of Fig. 2.3(a) while the feed-forward model of Fig. 2.3(b) yields convergence for $\left|kA_V\right| > 1$. Both models oscillate with constant amplitude in the case of $\left|kA_V\right| = 1$. Complications may arise for finite A_V as transient impedances depend on the time step: $Z_C=\Delta t/C$ for capacitors and $Z_L=L/\Delta t$ for inductors.

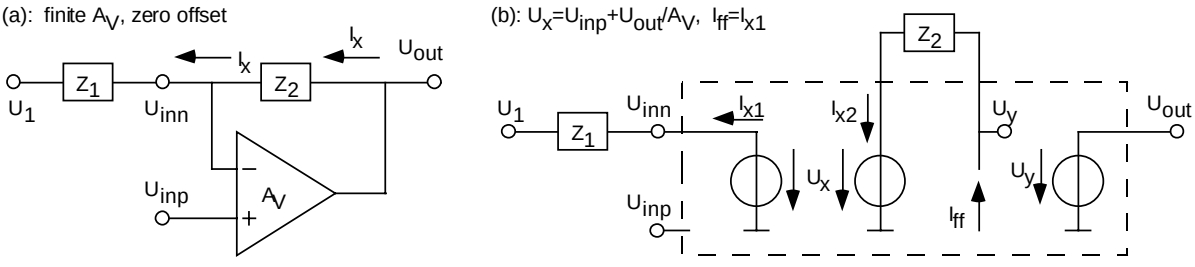


Figure 2.3: (a) OpAmp with finite amplification A_V, (b) behavioral feed-forward model.

Fig. 2.4 illustrates the ranges of stability for the two models of the operational amplifier shown in Figs. 2.3 (a) and (b).

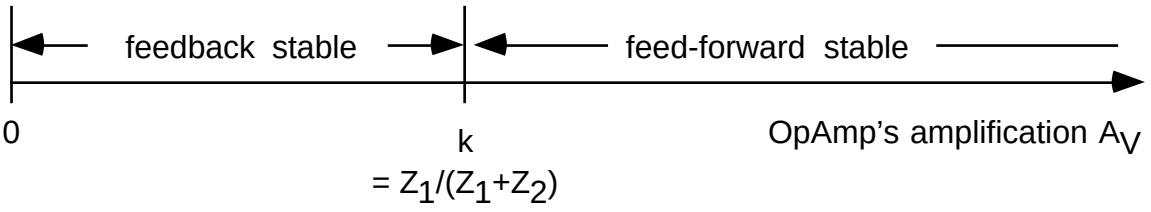
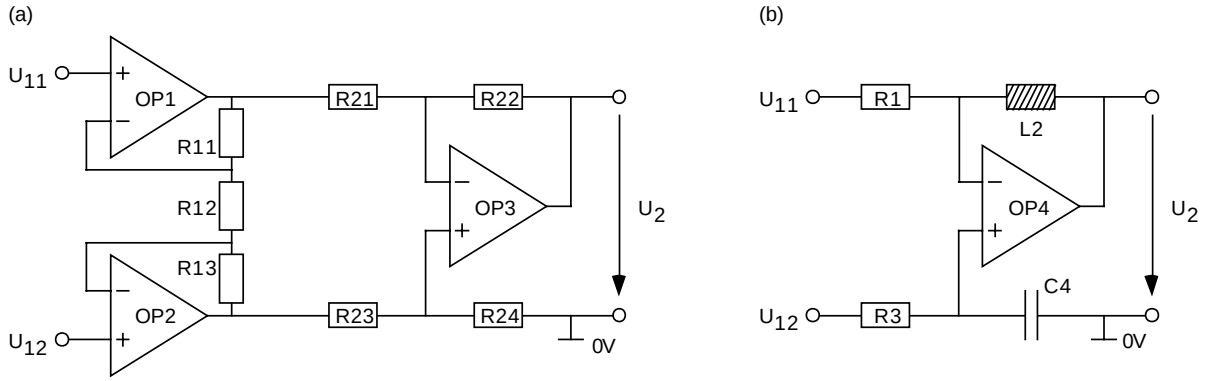


Figure 2.4: Stability ranges for the two models in Fig. 2.3 (a) and (b).

3 Applications

3.1 Differential-In, Single-Ended-Out Amplifiers Using RLC Networks

Fig. 3.1(a) presents a well known differential-in single-ended-out amplifier. All three OpAmps use the same ideal OpAmp model. The feedback network is resistive.
Fig. 3.1(b) shows a differential-in, single-ended-out amplifier using a network.
The simulations for these amplifiers are stable and the results close to Spice simulations.



(a) Three OpAmps, resistive network, (b) One OpAmp with RLC network.

Figure 3.1: Differential-in single-ended-out amplifiers using ideal OpAmp models.

3.2 Active RC Filter

Figure 3.2:

Active RC filter ideal OpAmp model.
Amplification:

Low frequencies: $-\frac{R_{21}+R_{22}}{R_{11}+R_{12}}$

High frequencies: $-\frac{R_{21}}{R_{11}}$

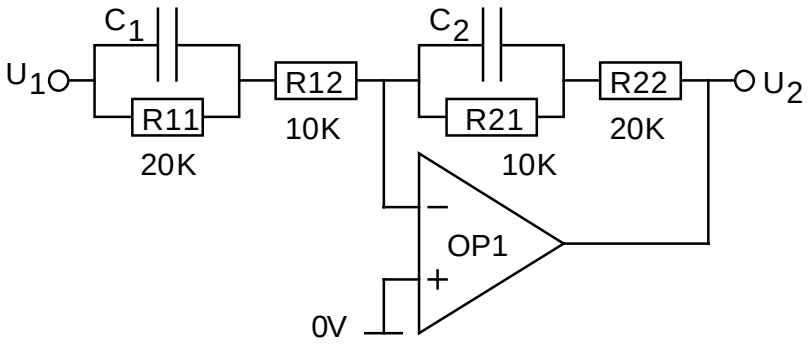


Fig. 3.2 shows an active RC filter. The OpAmp model is again assumed to be ideal. Low frequencies are blocked by the capacitors and amplified with a gain of $-(R_{21}+R_{22})/(R_{11}+R_{12})=-1$. High frequencies see the capacitors as short circuit and are amplified with a gain of $-R_{21}/R_{11}=-2$. So for a step response a peak amplification of -2 is expected which then decays to -1. While the peak was simulated correctly the simulation of the decay was still problematic when writing this paper.

3.3 Limitations

The differentiator in Fig. 3.3(a) uses an active integrator as feedback network. Though $U_{inn}=U_{inp}$ the feedback goes to the positive input of OP1 and the input impedance is infinite, which makes things difficult for the presented model. Fig. 3.3(b) shows a Schmitt trigger with feedback to the positive input of the OpAmp and $U_{inn}\neq U_{inp}$ is a normal situation. The circuits of Fig. 3.3 cannot be simulated with the OpAmp model detailed above.

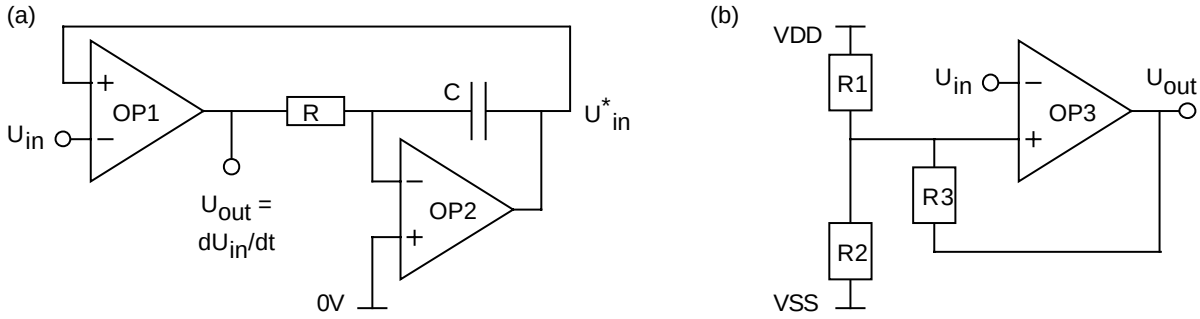


Figure 3.3: Circuits that cannot be simulated with the presented OpAmp model

4 Conclusions

Event-driven mixed analog-digital signal modeling is a method intended to simulate small portions of analog circuitry within a digital environment using the same event-driven simulation kernel. The development of a stable model for high gain feedback loops allowing for the use of operational amplifiers significantly increases the range of possible applications. The problems of adaptive time stepping and the treatment of non-linear devices is still unsolved. A method for adaptive time stepping will be proposed soon. A closed theory for non-linear devices is not yet available. This method of concurrent iteration reflects reality, where a network's node has no more information about the entire circuit than obtainable from connected pins and ports.

5 Acknowledgments

I would like to thank Mr. Ernst Bartsch for his skillful application of the presented devices in circuits and for many valuable hints resulting from his work and Prof. Gareth Monkman for reading the manuscript and providing useful advice.

6 References

[1] M. Schubert, „Verfahren zur Simulation von Netzwerken auf einer ereignisgesteuerten Zeitachse mittels verteilter, lokaler Iteration“, German Patent No. 19651502.5, 11. December 1996.

[2] M. Schubert, “Mixed Signal Modeling in VHDL by Distributed Local Iteration“, VHDL Form, Toledo, Spain, April 20-24, 1997.

[3] M. Schubert, “Mixed Analog-Digital Signal Modeling Using Event-Driven VHDL“, X Brazilian Symposium on Integrated Circuit Design - SBCCI’97, Porto Alegre, Brazil, August 25-27, 1997.

[4] E. Bartsch, M. Schubert, “Mixed Analog-Digital Circuit Modeling Using Event-Driven VHDL“, IEEE International Workshop on Behavioral Modeling and Simulation - BMAS’97, Washington D.C., USA, October 20-21, 1997.

[5] D.Thelen, J. MacDonald, “Simulating Mixed Analog-Digital Circuits on a Digital Simulator“, Proc. ICCAD-88, pp. 254-257, Nov. 1988.

[6] R. A. Cottrell, “Event-Driven Behavioural Simulation of Analogue Transfer Functions“, EDAC 1990, Glasgow, Scotland, 12-15 March 1990, pp. 240-243.

[7] F. Pichon, S. Blanc, B. Candaele, “Mixed-Signal Modelling in VHDL for System-on-Chip Applications“, ED&TC 1995, Paris, France, March 6-9, pp. 218-222.

[8] M. Declercq, M. Schubert, F. Clément, "5V-to-75V CMOS Output Interfaces", Proceedings of the1993 ISSCC, paper TP10.6, pp. 162-163 and 283, San Francisico, California, Feb. 24-26, 1993.

[9] M. Declercq, F. Clément, M. Schubert, A. Harb, M. Dutoit, "Design and Optimization of High-Voltage CMOS Devices Compatible wih a Standard 5V CMOS Technology", CICC, May 9-12, 1993.

[10] R. Boylestad, Electronic Devices and Circuit Theory, Prentice Hall, ISBN 0-13-394552-9.