Quick-Starting *ModelSim* for Electronics Lab Simulations

Abstract. This communication teaches a fast start to get *ModelSim* simulations for practical trainings in the *Electronics Laboratory* of *OTH Regensburg*.

1 Introduction

There are several labs and exercises using VHDL on FPGA boards on the homepage [Labs] of Prof. Schubert, Electrocnics Labs of OTH Regensburg [OTH].

Most VHDL users tend to synthesize and download VHDL code as soon as possible. But complicated errors are best detected by debugging the code in a simulator. Therefore, the Labs are accompanied by simulation models. They use the synthesizable files plus particular testbenches, that are found in subdirectory .\Models_DCDCbuck\VHDL\ModelSim\ of [zip].

Actually, the dominant board used during the practical trainings is Terasic's DE1-SoC board [DE1], equipped with an Intel Cyclone-V FPGA [CycV] and an *LTC2308* [AD] ADC featuring a maximum sampling rate of 500 Kilo-Samples per second (KSPS).

The Software Tools used in the laboratory are the *ModelSim* simulator and *Quartus*, used for syntheziser and download into the FPGA. Sufficient "light" versions are available free of charge [Q+M]. In the lab, we use version 18.1. Later versions are available for more powerful FPGAs. However, they require significantly more memory to support FPGAs that we do not use.

The structure of this document is as follow:

Chapter 1: this introduction
Chapter 2: Getting Started with *ModelSim* for Electronics Labs of OTH Regensburg
Chapter 3: Operating the *ModelSim* Simulator
Chapter 4: Summary
Chapter 5: References

2 Getting Started with *ModelSim* for Electronics Labs

Download on [Labs] the *DCDCbuck_Rev#* (with #=5, 10 or 11) zip file [zip] from

Board DCDCbuck_Rev. 5: VHDL_Files_4_Labs, VHDL_Files_4_Labs_until_Oct2021
Boards DCDCbuck_Rev.10 + 11: Files_4_Labs, boards DCDCbuck_Rev. 10 and 11,

Herinafter we will assume that you downloaded *Rev10 and 11* files. (The Rev.5 package omits the highest directory level.) Unzip the package and navigate to subdirectory
.\Models_DCDCbuck\VHDL\ModelSim\tb_de1soc_DCDCbuck_pcb00.

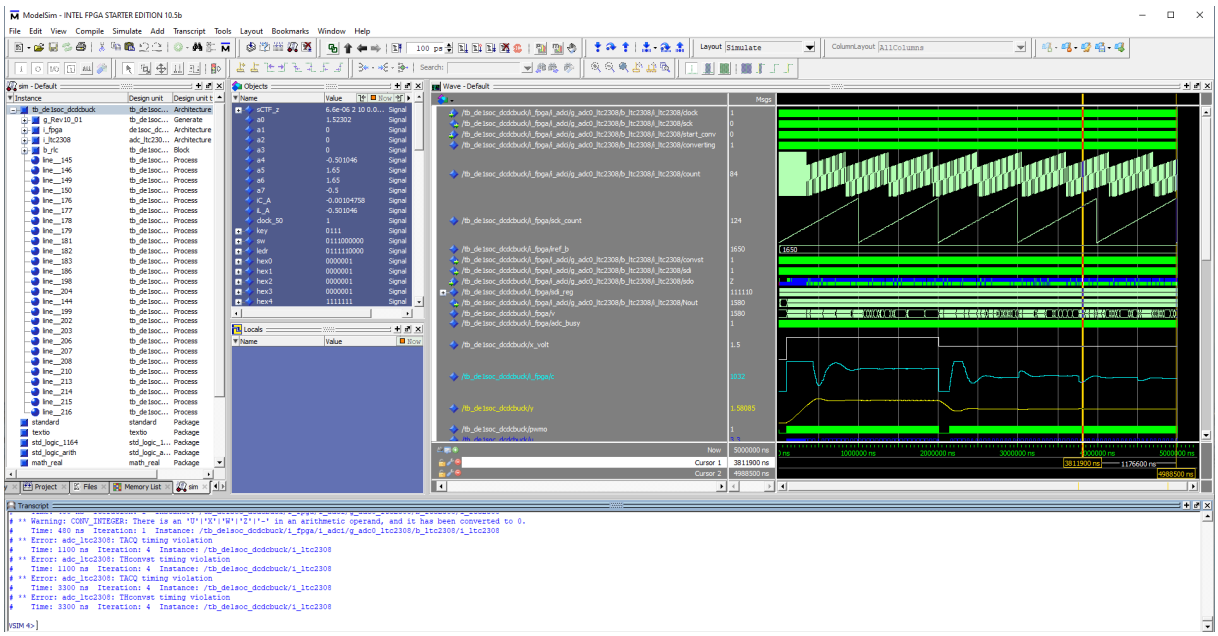
In subdirctory "*\tb_de1soc_DCDCbuck_pcb00*", which assumes the theretical board *pcb00* with ideal device parameters, you will find the following 4 files:

tb_de1soc_DCDCbuck.vhd	VHDL testbench
wave.do	script file declaring the graphics window
work.do	script file running the complete simulation
wstart.mpf	*ModelSim* project file, starting and initializing *ModelSim*.

1. Double-click left on file *wstart.mpf*. The ModelSim simulator should start. Type *ls* (list directory) into the *transcript* window to see the 4 files listed above, confirming that *ModelSim* is set in this directory *tb_de1soc_DCDCbuck_pcb00* as working directory.

   Alternatively, you can start *ModelSim* from the *Windows* start menu, close all upcoming windows and select your working directory from the menu bar: *File → Change Dirctory → ... \tb_de1soc_DCDCbuck_pcb00.*

2. Type the command "*do work.do*" into the *ModelSim transcript* window. Then, the simulation should start and run until you see the screen in Fig. 2.



3 Operating the *ModelSim* Simulator

The ModelSim simulator can be operated by both menu and commands in the *transcript window*. Commands use the syntax of the Tool command language [Tcl]. The key advantage of using commands is that they may be summarized in a script file, hereinafter featuring the extension **.do*. Several command can be processed by invoking the script file with keyword *do*. As an example we operated the ModelSim typing

do work.do

into the transcript window in "Chapter 2: Getting Started with *ModelSim*". Open file work.do with an ASCII [ASC] (unformatted text) editor to see the *Tcl* command lines.

Using script command files

Note that do-files may be nested, i.e. do-file may invoke do-files: *work.do* for example contains the command line "*do wave.do*", which executes the *wave* (graphics) window.

Relative addressing

Acc. to Linux [Linux] and UNIX [Unix], a single and double dot as directory names stand for

.	actual working directory
..	parent directory of actual working directory

Application examples:

./*subdir1*	subdirectory *subdir1* of the actual working directory
../..	parent directory of parent directory of actual working directory
../*subdir2*	subdirectory *subdir2* of parent directory of actual working directory

Debug the *VHDL* code

In the Instance *window*, select index tab "*sim*" and navigate to the VHDL module of your interest. The belonging VHDL source code will be displayed in the editor window, and the actual ontents of data objects will be displayed in the *Objects* window. Click on the blue arrows (*step into, step over*,…) in the ModelSim menu bar to debug your code line by line. Click on a data object in the objects window and draw it into the graphics (*wave*) window to make its waveform visible versus time. Resimulate to see the values of a new signal in the *wave* window. Do not forget to save its format before resimulation.

Operating the Graphics Window

The graphics (*wave*) window should be formatted interactively, to act and correct it to get what you want to see. You can draw signals from the *Objects* window into the wave window. To see the values of the objects, you will have to simulate again. After simulation you actual graphics formating will be lost if you do not save it. To save the Graphics window structure, click on the *Save* menu-button while the *wave* window is active. (Click into the *wave* window to make it active.) Then *ModelSim* writes/overwrites file *wave.do* in your actual working directory. Click on signals in the wave window and the select properties with right mouse button to format them.

4 Summary

This document details how to use pre-prepared *ModelSim* files for the simulation of VHDL code of the *Electronics Lab* at *OTH Regensburg*.

5 Refenreces

[Labs] https://hps.hs-regensburg.de/~scm39115/homepage/education/labs/Lab_ElectronicBoards/Lab_ElectronicBoards.htm
[OTH] https://www.oth-regensburg.de/
[zip] https://hps.hs-regensburg.de/~scm39115/homepage/education/labs/Lab_ElectronicBoards/Models_DCDCbuck_R10.01.04.zip
[De1] https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&No=836
[CycV] https://www.intel.de/content/www/de/de/products/details/fpga/cyclone/v/gt.html
[AD] https://www.analog.com/en/products/ltc2308.html
[Q+M] https://hps.hs-regensburg.de/~scm39115/homepage/education/labs/Lab_ElectronicBoards/Download+Installation_of_Quartus+ModelSim_v18.1.pdf
[Tcl] https://de.wikipedia.org/wiki/Tcl
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