Getting Started With *DSM* Grandchild Board

Using VHDL

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Getting Started With *DSM* Grandchild Board Using VHDL

Abstract. This communication presents the DSM conversion grandchild board, which is a daughter board to the *ADA* board, which is a daughter board to different *DE1-SoC* board or other *DEx* boards from *Terasic* with compatible user header, e.g. *DE2, DE2-70, DE2-115*.

1 Introduction

1.1 Objectives and Organization of this Document

This document illustrates how the A/D Converter (ADC) and D/A Converters (DAC) on the *ADA* board can be assembled to form a delta-sigma ($\Delta\Sigma$) modulator (DSM) operating as ADC. This dommunication is focused to the analog part of the $\Delta\Sigma$ ADC. The significantly more complex digital part is given by the author.

This document assumes that you are familiar with the *DE1-SoC* board or a similar *DEx* board and the *ADA* daughterboard that carries the *DSM* board. The required introductions *Getting Started with DE1-SoC Board* and *Getting Started with ADA Daughter Board* are available from the author's homepage [15].

The organization of this document is as follows:

Section **1** is this **introduction**,
Section **2** makes the user familiar with the *DSM* board **hardware**,
Section **3** introduces first tests with the *DSM* board using **software**,
Section **4** assembles a $\Delta\Sigma$ A/D/A conversion system with *ADA* and *DSM* boards,
Section **5** draws relevant **conclusion** and
Section **6** offers **references.**

1.2 Tools

1.2.1 *DE1-SoC* Hardware

This document assumes that you are familiar with the *Terasic's* [2] *DE1-SoC* board using an *Intel Cyclone V FPGA* [2] or a similar board *DEx* board with the same general-purpose input/output (GPIO) user header. The version of your *DE1-SoC* board can be identified at [3]. *DE1-SoC* board revisions *F* and *G* differ in a printed company label only. To get it from the internet, go to [4] to find and download *DE1-SoC_v.5.1.2_HWrevF_SystemCD.zip* [5] or a later version and download it. It contains amongst other things important documents such as *DE1-SoC User Manual* [6] and *Schematic* [7]. On the computer system of OTH Regensburg you will also find the CD on drive K:\Sb\ [8]. Do not use any other manual revision to follow this documentation. The differences are sometimes considerable.

1.2.2 *Quartus II* [9] and *ModelSim* [10] Software Tools

It is assumed that you have *Intel's ModelSim [10] and Quartus II 13 [9]* software available. To download this freeware for your private PC you have to sign in at *Intel* [11]. At OTH Regensburg's PC pools of faculties *EI* and *IM* this software is installed. At faculty *EI* also *Quartus II 8* is installed supporting the older *DE2* boards with *Cyclone II* FPGAs, because they are no longer supported for *Quartus II* versions greater than 13.1.

1.2.3 Use of *VHDL*

The *IEEE standard VHDL Language reference manual* [12] is difficult to read. *Qualis VHDL Quick Reference Card* [13] and *1164 Packages Quick Reference Card* [14] are compact but difficult to understand. Feel free to find your own sources.

VHDL is not case sensitive. In the following, **KEYWORDS** will be written in **ALL CAPITAL LETTERS** and user defined names in **lowercase letters**. Exception: Capitalized initials are used for composed self-made names, e.g. *AddressBus* or *DataBus*. Self-made data types begin with *t_*, e.g. *t_StateVector*.

1.3 Acknowledgements

The author would like to thank *Terasic Technologies* [1] for admission to use screen copies of *Terasic* documentation for teaching purposes in this lectures.

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At 19.09.2014 08:49, Terasic - Dong Liu wrote:
   Dear Martin,
   Thank you for using DE boards to teach VHDL. Yes, you can open all
   DE design resources for teaching purpose. Thank you!
   Best Regards,
   Doreen Liu
```