Getting Started With *DE1-SoC* Board

Using VHDL

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Abstract. This communication teaches first step to operate Terasic's *DE1-SoC* board using an Intel *Cyclone V* FPGA.

1 Introduction

1.1 Objectives and Organization of this Document

This document is intended as introduction for students at OTH Regensburg that use the *DE1-SoC* board in some way.

The organization of this document is as follows:

Section **1** introduction,
Section **2** makes the user familiar with starting the *DE1-SoC* board at OTH Regensburg,
Section **3** gives some more detailed insight into the *DE1-SoC* board hardware,
Section **4** provides a first understanding of a VHDL code,
Section **5** demonstrates how to save a result as new project,
Section **6** summarizes the document and
Section **7** lists references.

1.2 Acknowledgements

The author would like to thank *Terasic Technologies* [1] for admission to use screen copies of *Terasic's* documentation for teaching purposes in this lectures.

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At 19.09.2014 08:49, Terasic - Dong Liu wrote:
  Dear Martin,
  Thank you for using DE boards to teach VHDL. Yes, you can open all
  DE design resources for teaching purpose. Thank you!
  Best Regards,
  Doreen Liu
```

1.3 Tools

1.3.1 *DE1-SoC* Hardware

The course makes you familiar with the *Terasic's* [2] *DE1-SoC* board using an *Intel Cyclone V FPGA* [2]. Identify the version of your board [3].

What is the revision letter of your hardware board? **F**

. . . . . .

Hint: Revisions *F* and *G* differ in a printed company label only. To get it from the internet, go to [4] to find and download *DE1-SoC_v.5.1.2_HWrevF_SystemCD.zip* [5] or a later version and download it. It contains amongst other things important documents such as DE1-SoC User Manual [6], [18] and Schematic [7], [19]. The latest available Version is *Rev .F*. On the computer system of OTH Regensburg you will also find the CD on drive K:\Sb\ [8]. Do not use any other manual revision to follow this documentation. The differences are sometimes considerable.

1.3.2 Quartus [9] and ModelSim [10] Software Tools

It is assumed that you have *Intel's ModelSim and Quartus* software available. To download this freeware for your private PC you have to sign in at *Intel* [11]. At *OTH Regensburg's* PC pools of faculty *EI* this software is installed.

1.3.3 Use of VHDL

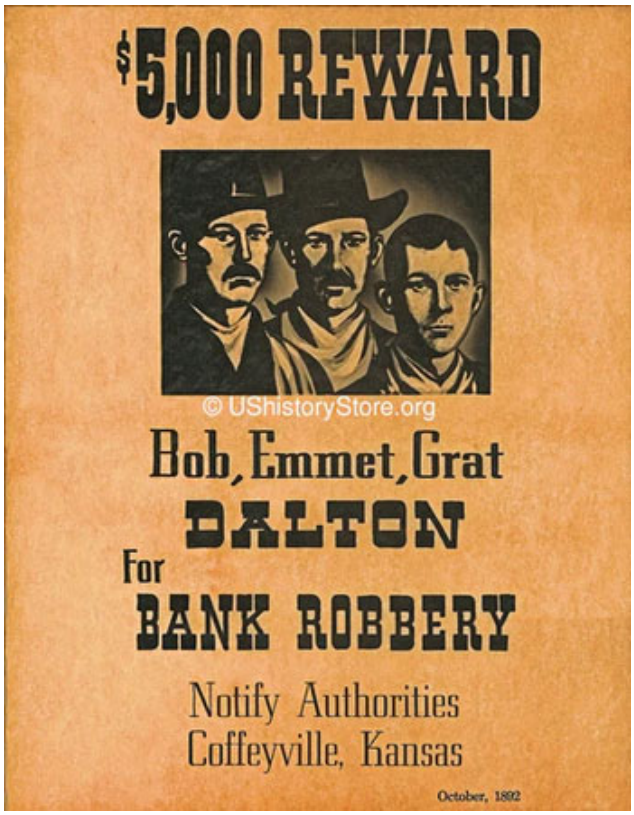
The *IEEE standard VHDL Language reference manual* [12] is difficult to read. Qualis VHDL Quick reference Card [13] and 1164 Packages Quick reference Card [14] are compact but difficult to understand. Feel free to find your own sources.

VHDL is not case sensitive. In the following, **`KEYWORDS`** will be written in **`ALL CAPITAL LETTERS`** and user defined names in **`lowercase letters`**. Exception: Capitalized initials are used for composed self-made names, e.g. *AddressBus* or *DataBus*. Self-made data types begin with *t_*, e.g. *t_StateVector*.

1.4 Wanted: Bounty Hunters!

1 bounty for reporting an error in the author's documentation that he is not yet aware of.

The bounty will be paid regardless of whether the script is presented torn or intact.



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Regensburg, Bavaria

2 Getting Started

Goal of this subchapter is to get started with the *DE1-SoC* board and *Quartus* [6] software on the computer system of *OTH Regensburg*.

2.1 Getting Started with the *DE1-SoC* Hardware

Note for all the text below: It is *DE(one)-SoC* hardware, not *DEL-SoC*!

Requirements: have available

- Hardware: *DE1-SoC* board,
- Software: *Quartus* 18 or later installed on your computer,
- Documents from *DE1-SoC_v.5.1.2_HW_RevF_SystemCD.zip*: *UserManual\DE1-SoC_User_manual.pdf, Schematic\DE1-SoC.pdf.*

Take your *DE1-SoC* board, plug in the 12 V_{DC} power supply and connect the USB port with your computer. Press *Power ON/OFF* button. You should see some red light emitting diodes (LEDs) blinking and the 7-segment display counting hexadecimal numbers from 0 … F.

Note how we display hex-numbers 6: 6 , 8: 8 , B: b
with 7 bars like on the 7-seg display . . . .

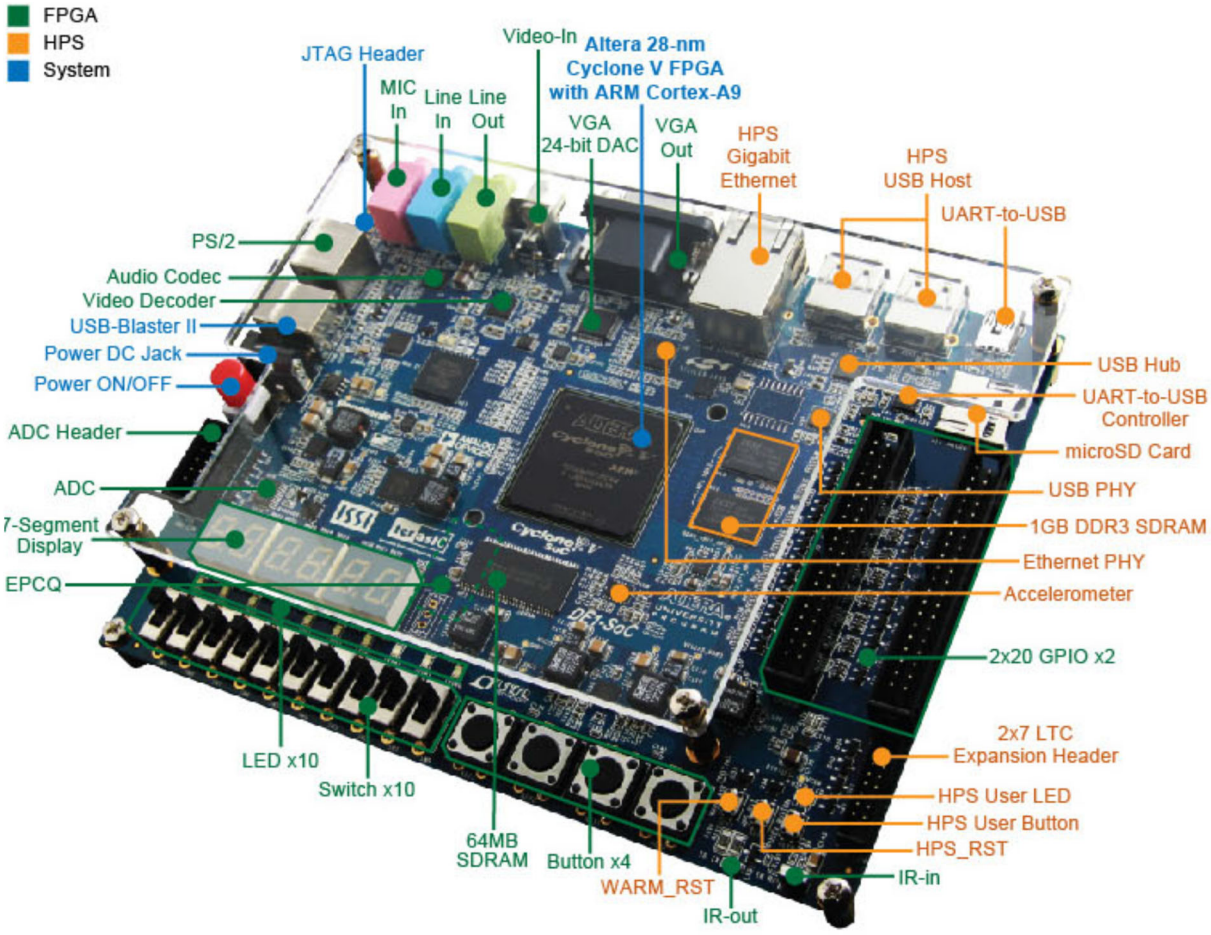

Fig. 2.1: *DE1-SoC* board (copied from *DE1-SoC Quick Start Guide*, document *DE1-Soc_QSG.pdf* in *DE1-SoC_v.5.1.2_HW_RevF_SystemCD.zip* [4]).