Getting Started With *ADA* Daughter Board

Using VHDL

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Abstract. This communication presents the *ADA* conversion board, which is presented as daughter board to DE1-SoC board, but is compatible with different *DEx* boards from *Terasic*, featuring the required 40 pin user header, e.g. *DE2, DE2-70, DE2-115*.

1 Introduction

1.1 Objectives and Organization of this Document

This document is intended for students learning time-discrete Signal processing, A/D and D/A conversion as well as electronic design automation using VHDL. It is a comprehensive example that teaches different aspects on the same system.

Naming conventions. Digital signal names containing strings *din* (digital in) or *dout* (digital out) respect the *ADA* board point of view. Signal *DAC3dout9* is a 9-level digital output signal from the *ADA* board and input to *DAC3*. Signal *adc_din* is output from the *ADC* and a digital input signal to the *ADA* board.

The organization of this document is as follows:

Section **1** is this **Introduction**,
Section **2** introduces the **A/D/A conversion board** used as example,
Section **3** presents the most important A/D and D/A conversion models,
Section **4** tests the DACs
Section **5** tests the flash ADC
Section **6** tests the flash ADC followed by DAC3 and measures quantization noise
Section **7** draws relevant **conclusions** and
Section **8** offers **references.**

1.2 Tools

1.2.1 *DE1-SoC* Hardware

This document assumes that you are familiar with the *Terasic's* [1] *DE1-SoC* board using an *Intel Cyclone V FPGA* [2] or a similar *DEx* board with the same general-purpose input/output (GPIO) user header. The version of your *DE1-SoC* board can be identified at [3]. *DE1-SoC* board revisions *F* and *G* differ in a printed company label only. To get it from the internet, go to [4] to find and download *DE1-SoC_v.5.1.2_HWrevF_SystemCD.zip* [5] and download it. It contains amongst other things important documents such as *DE1-SoC User Manual* [6] and *Schematic* [7]. On the computer system of OTH Regensburg you will also find the CD on drive K:\Sb\ [8]. Do not use any other manual revision to follow this documentation. The differences may be considerable.

1.2.2 *Quartus II* [9] and *ModelSim* [10] Software Tools

It is assumed that you have *Intel's Quartus II 13 [9]* and *ModelSim [10]* software available. To download this freeware for your private PC you have to sign in at *Intel* [11]. At OTH Regensburg's PC pools of faculties *EI* and *IM* this software is installed. At faculty *EI* also *Quartus II 8* is installed supporting sme older *DE2* boards with *Cyclone II* FPGAs, because they are not supported for *Quartus II* versions greater than 13.1.

1.2.3 Use of *VHDL*

The *IEEE standard VHDL Language reference manual* [12] is comprehensive and demanding to read. *Qualis VHDL Quick Reference Card* [13] and *1164 Packages Quick Reference Card* [14] are compact but difficult to understand. Feel free to find your own sources.

VHDL is not case sensitive. In the following, **`KEYWORDS`** will be written in **`ALL CAPITAL LETTERS`** and user defined names in **`lowercase letters`**. Exceptions are capitalized initials used for composed self-made names, e.g. *AddressBus* or *DataBus*. Self-made data types begin with *t_*, e.g. *t_StateVector*.

1.3 Acknowledgements

The author would like to thank *Terasic Technologies* [1] for admission to use screen copies of *Terasic* documentation for teaching purposes in this lectures.

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At 19.09.2014 08:49, Terasic - Dong Liu wrote:
  Dear Martin,
  Thank you for using DE boards to teach VHDL. Yes, you can open all
  DE design resources for teaching purpose. Thank you!
  Best Regards,
  Doreen Liu
```

2 The *ADA* Daughter Board

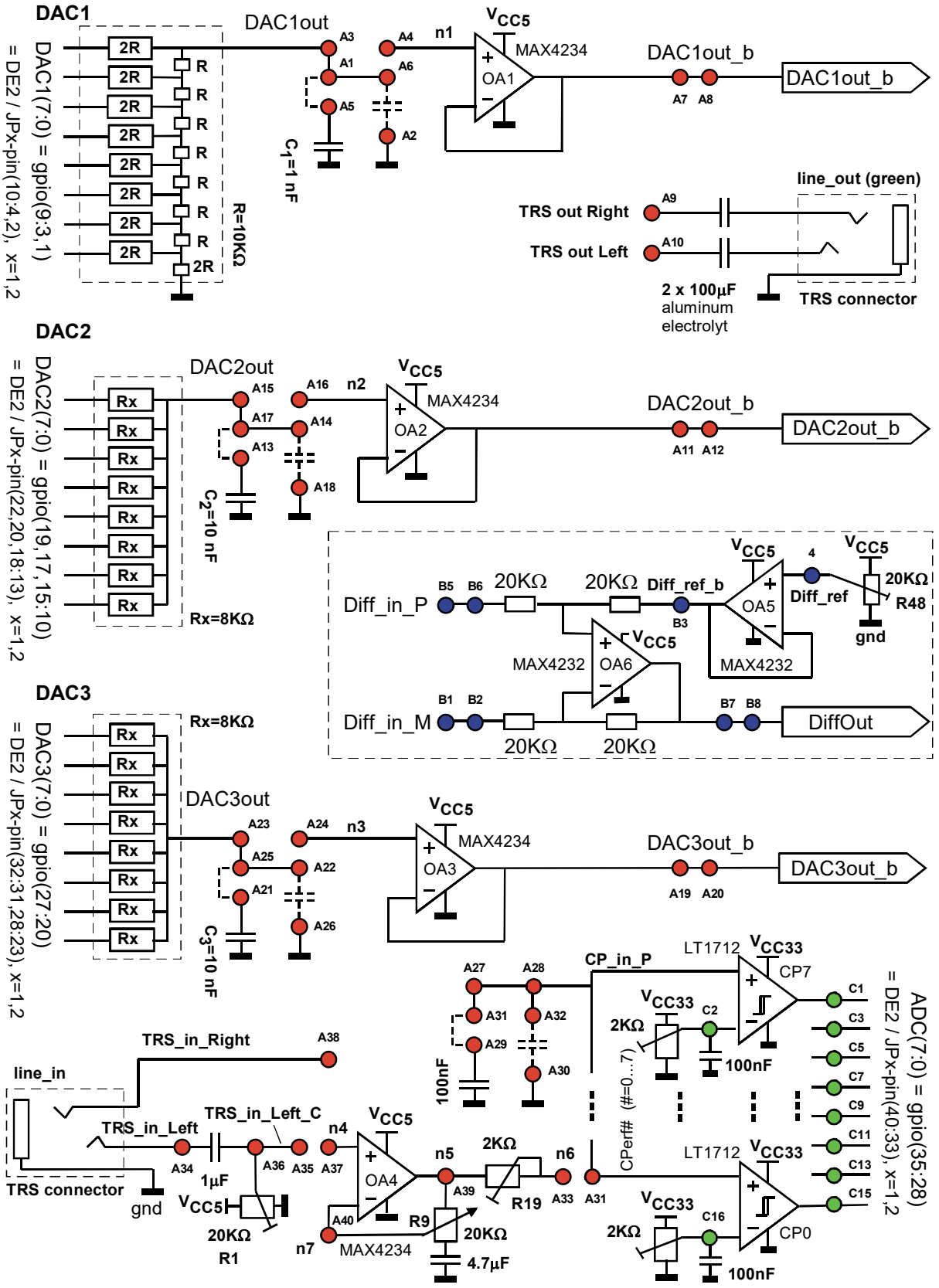


Fig. 2.1: Schematics of the *ADA* daughter board

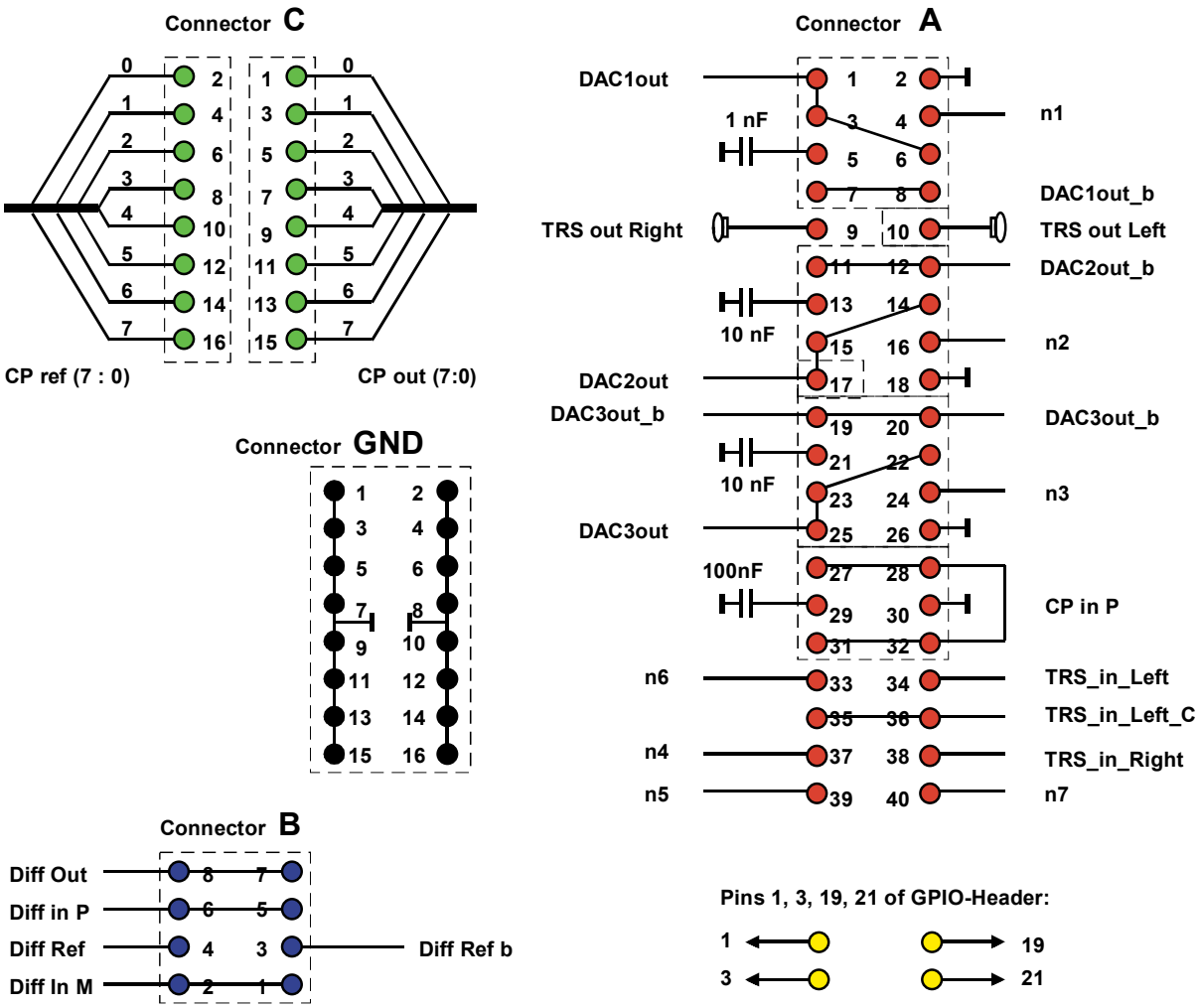
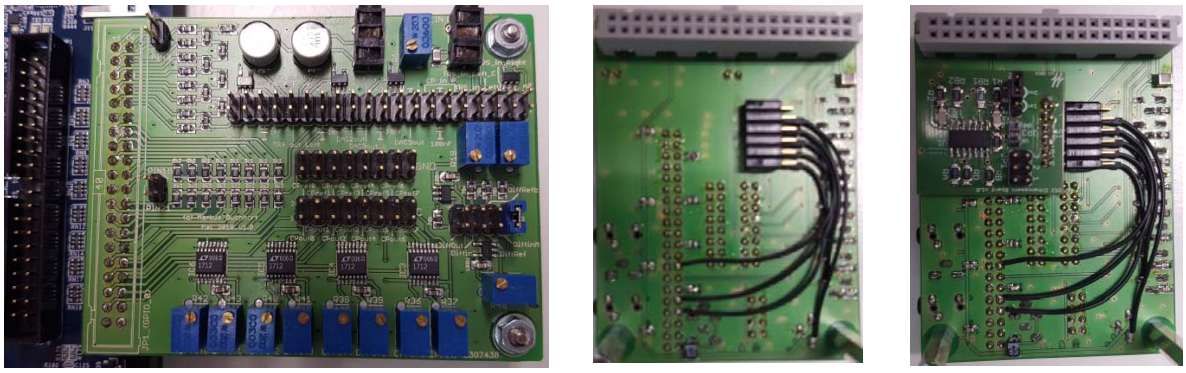


Fig. 2.2: Connectors of the *ADA* daughter board



(a) top view, plugged *DE1-SOC* board (b) bottom view (c) with *DSM* board

Fig. 2.3: ADA daughter board photos

- Fig. 2.1 shows the *ADA* daughter board schematics.
- Fig. 2.2 illustrates the *ADA* board from the user header connector point of view.
- Fig. 2.3 shows photos of the *ADA* board with and without *DSM* grandchild board.

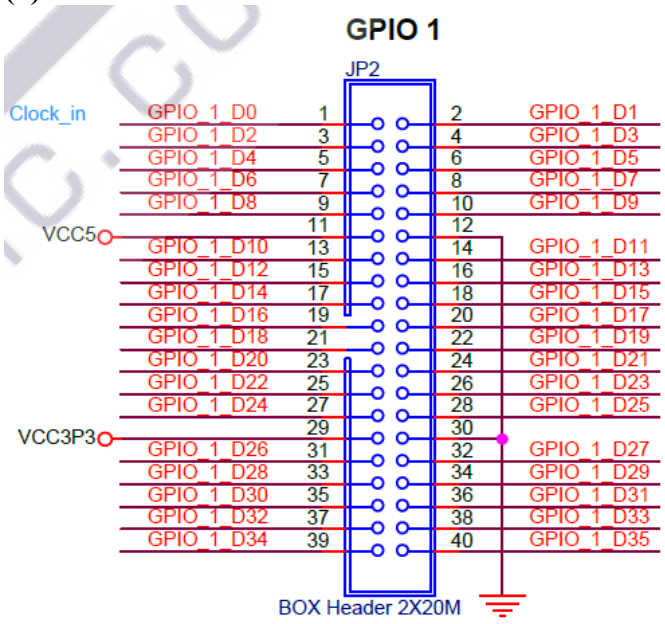
- Fig. 2.4 is related to the user headers of different *DEx* boards and maps the GPIO labels to the user header connector pins.
- Fig. 2.5 shows the production schematics of the *ADA* board with DAC schematics on the top part and other schematics on the bottom part of the figure.
- Fig. 2.6 the production layouts in top and bottom view, respectively.

Deactivate the *DSM* grandchild board under the *ADA* daughter board to avoid inferences when working with this document. This may be done in different ways, for example:

- Completely disconnect *DSM* grandchild board from *ADA* board → please be careful not to lose the small *DSM* board.
- Plug grandchild board into the unconnected parking position of the plug on the *ADA* board, which is the row with the bigger distance to the *ADA* board.

This tutorial is made for the *DE1-SoC* board. The user-header pins are assigned for compatibility to *DE2, DE2-70* and *DE-115* boards. Therefore pins 1, 3, 19, 21 of the user header remain unused. Figs. 2.4(a) copied from the *DE1-SoC* board's schematics [7] illustrates the user header's connectivity, while Fig. part (b) copied from the user manual [6], shows the current limitations of the on-board voltage sources V_{CC3P3} and V_{CC5}.

(a) User header of *DE1-SoC b*oard



(b) Current limitations

Supplied Voltage	*Max. Current Limit*
5V	1A
3.3V	1.5A

Fig 2.4: *De1-SoC* user header *JP1*:
(a) Schematics copied from [7]
(b) Current limitations, copied from [6]

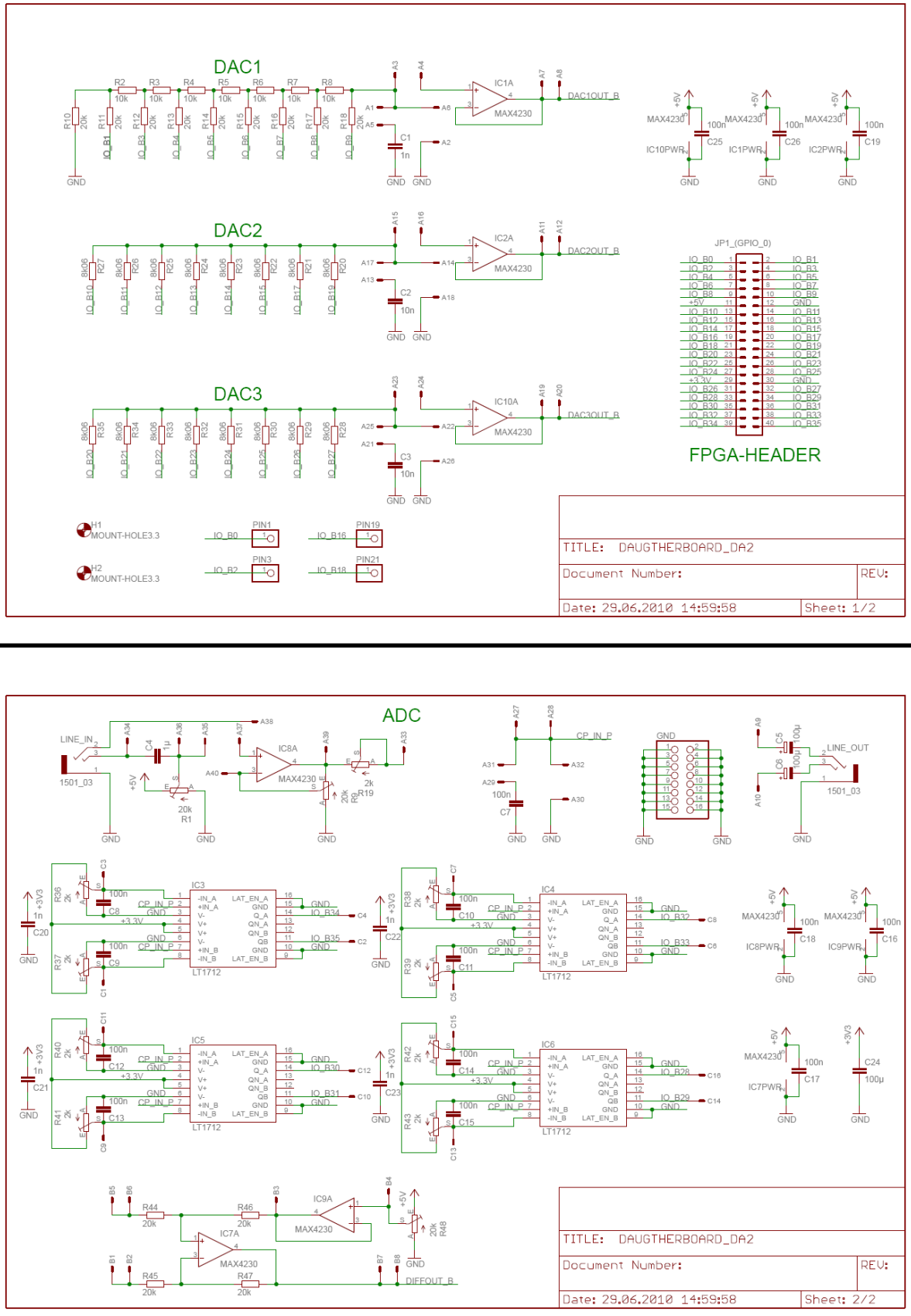


Fig. 2.5: *ADA* board schematics (by Markus Buchhart, 2010)

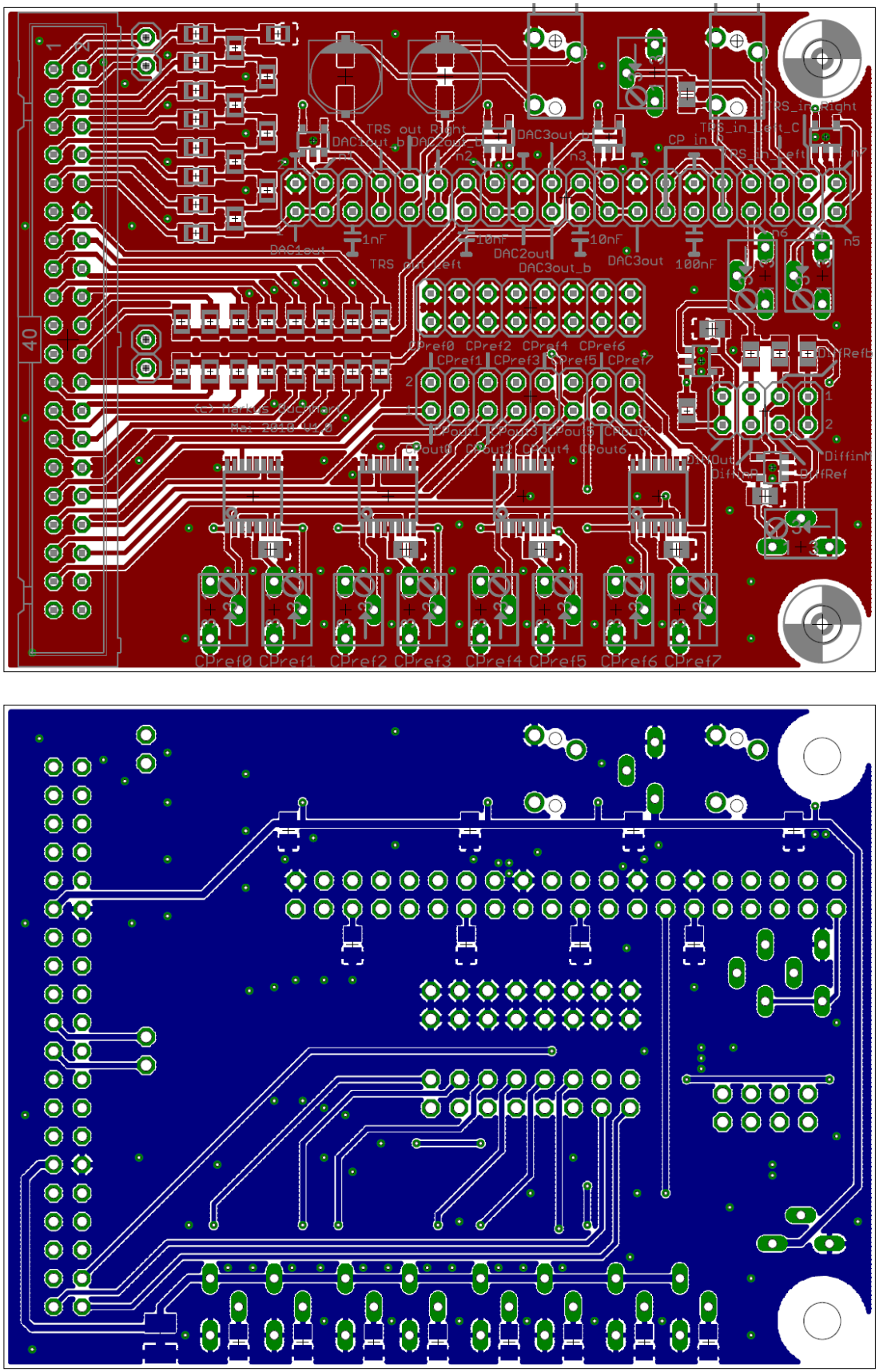


Fig. 2.6: *ADA* board **(red)** top and **(blue)** bottom layer layout (by M. Buchhart, 2010)

3 A/D and D/A Converter Modeling

Chapter 3.1 offer basic behavioral models of A/D and D/A conversion.
Chapter 3.2 models the flash DACs named *DAC2* and *DAC3* on the *ADA* daughter board.
Chapter 3.3 models the R2R DAC named *DAC1* used on the *ADA* daughter board

3.1 Basic Behavioral Models

We model a D/A converter (DAC) behaviorally as

$$U_{DAC,out} = \sum_{i=0}^{order} \Delta_i N_{DAC,in}^i$$

with $U_{DAC,out}$ and $N_{DAC,in}$ being output voltage and digital input word, respectively. According to signal processing linearity theorem, Δ_i=0 for $i \neq 1$, so that a linear DAC can be modeled as

$$U_{DACout} = \Delta_1 N_{in}$$

We model an A/D converter (ADC) behaviorally as

$$N_{ADC,out} = round\left(\sum_{i=0}^{order} \alpha_i U_{ADC,in}^i \right)$$

with $N_{ADC,out}$ and $U_{ADC,in}$ being digital output word and input voltage, respectively. According to signal processing linearity theorem, α_i=0 for $i \neq 1$, so that a linear ADC can be modeled as

$$N_{ADC,out} = round\left(\alpha_1 U_{ADC,in} \right).$$