# Debugging the DCDbuck_Rev10 Board

**Abstract.** This document gives some advice on what to do when a DC/DC buck board is not working properly.

## 1 Introduction and Contents

Sometimes we see that a PCB is not working properly. What actions can be taken to debug the board?

You have to understand the functionality of the board in order to be able to evaluate voltages and waveforms.

# 2 Debugging the *DCDCbuck* Board

## 2.1 System Setup

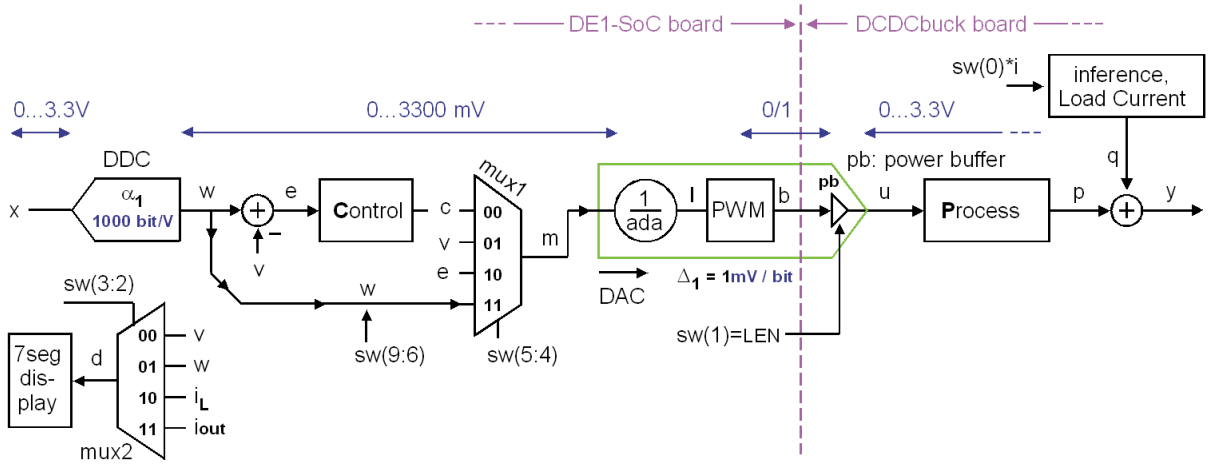



**Fig. 2.1:** The DC/DC buck converter setup.

Fig. 2.1 illustrates the top-level schematics of the DC/DC controller and illustrates the functionality of its switches:

| | |
|---|---|
| **`sw(9:6)`** | allow to set 15 different reference voltages in mV on signal *w* ("wanted"), setting "1111" refers to a reference voltage delivered by the hard processor system (HPS). |
| **`sw(5:4)`** | take a decision about which signal is used as input to the PWM-DAC. |
| **`sw(3:2)`** | take a decision about which signal is shown on the 7-segment display. |
| **`sw(1)`** | decides on synchronous ('1') or asynchronous ('0') operation. |
| **`sw(0)`** | enables a load current of 1A to be switched on ('1'). |

Set an output voltage of some 100mV > 1V, e.g. 1250V using **`sw(9:6)`** **`"0000"`**.

To debug the digital part of the DCDCbuck board, it makes sense to open the feedback loop, bypass the controller and put reference ***w*** directly at the input of the PWM modulator. To so, set the following switches (solutions see below):

**`sw(_____) = _____`** .

Display the output voltage ***v*** measured by ADC *LTC2308* on the 7-segment display

**`sw(_____) = _____`** .

Set synchronous operation and load current off:

**`sw(_____) = _____`** .

in summary, the overall switch setting is

**`sw(9:0) = _____`** .

**Solutions to chapter 2.1:** Setting of switches for this test:
To debug the digital part of the DCDCbuck board, it makes sense to open the feedback loop, bypass the controller and put reference ***w*** directly at the input of the PWM modulator. To so, set the following switches (solutions see below):
**sw( 5:4 ) = 1 1** .

Display the output voltage ***v*** measured by ADC *LTC2308* on the 7-segment display
**sw( 3:2 ) = 0 0** .

Set synchronous operation and load current off:
**sw( 1:0 ) = 1 0** .

in summary, the overall switch setting is
**sw(9:0) = 0000 11 00 10** .

## 2.2 Schematics for Testing the *LM27222*

### 2.2.1 First Tests

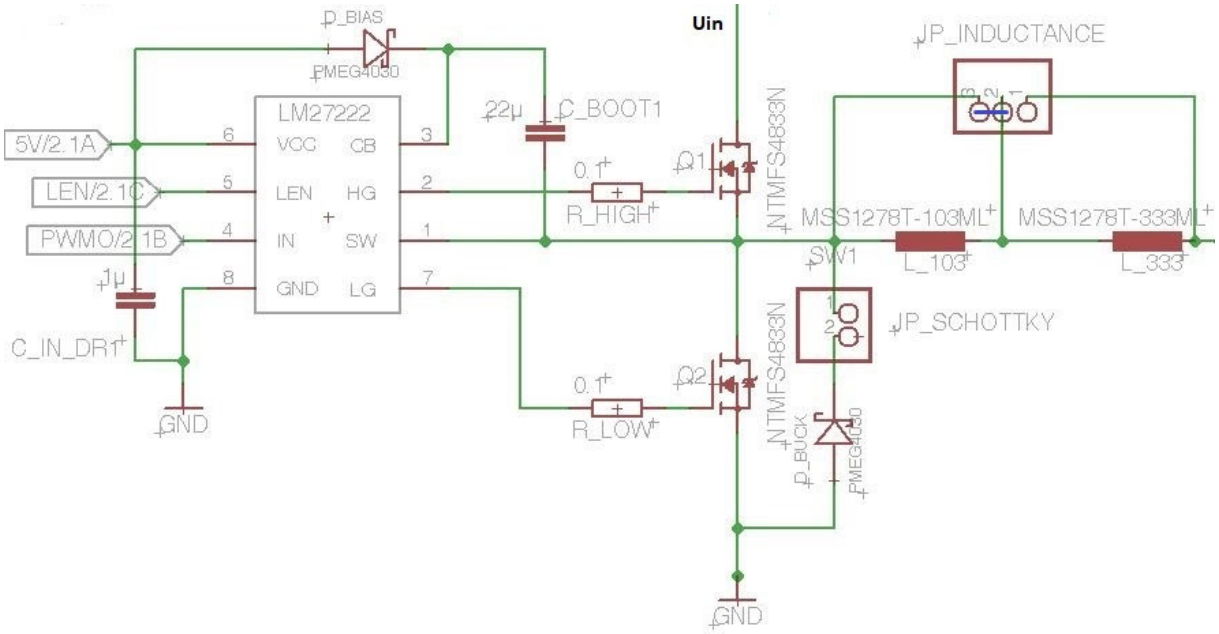



**Fig. 2.2.1:** The DC/DC buck converter schematics for LM27222 tests.

Only hold the board by the side edges. If you must touch devices on the board, do so with clean fingers and avoid touching conductive parts such as wireline pins. This is because human skin is covered in a layer of sweat, salt and fat. This can cause leakage currents between conductive elements.

1. Apply light bending stress to the board. This must not impair its function
2. Try pushing larger components back and forth a little. They should not wobble and these forces should not affect the functionality of the board.
3. During normal operation, no device should get so hot that you cannot touch it. Check the board under an infrared camera or touch critical devices carefully with clean fingers.

## 2.2.2 Checking voltages and signals with probe and Oscilloscope

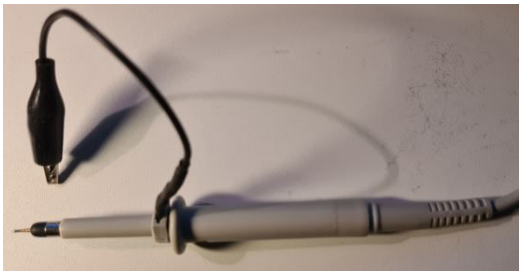


**Fig. 2.2.2:** Probe to be connected to the oscilloscope with a BNC plug. Be aware, that many probes have a built-in 1:19 voltage divider.

Use a probe as illustrated in Fig. 2.2.2, which is attached to your oscilloscope. Be careful to not cause short circuits between neighboring pins when touching LM27222 I/O pins with the probe.

Identify the *LM27222* chip on your DCDCbuck board. Identify pin 1 … pin 8 using the datasheet [LM27222].
[LM27222]: https://www.ti.com/lit/ds/symlink/lm27222.pdf?ts=1667637493881&ref_url=https%253A%252F%252Fwww.google.com%252F

Connect *CH1* of the oscilloscope with pin3 of JP1=gpio_0 user header of the *DE1-SoC* board. Connect *CH2* of the oscilloscope with pin1 of JP1=gpio_0 user header of the *DE1-SoC* board. (Check results with Figs. in chapter 2.3.) Verify with a probe at *CH3* that *LM27222's* …

- *pin8* = *gnd* = 0V % is the ground pin really connected to ground?
- *pin6* = $V_{CC}$ = 5V % is the VCC pin connected to 5V?
- *pin4* = *IN* = pin6 % should be identical to pwmo on CH2
- *pin7* = *LG* == (NOT(*pwmo*) AND LSE) % check LG. Note: *LSE* = *LEN* = *sw*(1)
- *pin2* = *HG* = $a_1 \cdot pwmo + a_0$, whereas $a_1 > 0$, $a_0 \geq 0$ % check *HG*
- *pin1* = *SW* = $a_1 \cdot pwmo + a_0$, whereas $a_1 > 0$, $a_0 \geq 0$ % check switching node *SW*
- *pin3* = *CB* = $a_1 \cdot pwmo + a_0$, whereas $a_1 > 0$, $a_0 \geq 0$ % check boots-trap node *CB*

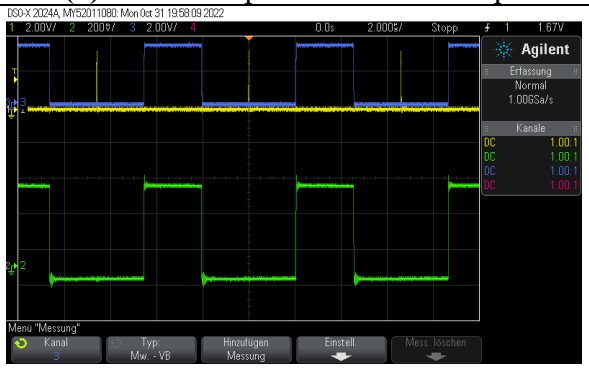
# 2.3 Checking Signals at Pins of *LM27222*

## 2.3.1 Check Control Signals *pwmo* (*IN*), Low-Gate (*LG*), High-Gate (*HG*)

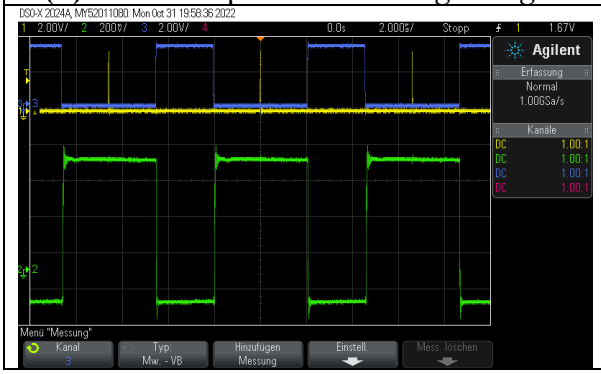
**Figure 2.3.1:** Signals, $U_{in}$=3.3V, $w$=1250mV

yellow: first bit of PWM interval, 0/3.3V
blue: PWM signal *pwmo* from the FPGA: delivers *centered '1'*, 0/3.3V
green: observed signal
(a) grn: PWM input signal (*FPGA's pwmo*) measured at pin4 of *LM2722*
(b) grn: Low-gate (*LG*) signal measured at pin7 of *LM2722*: inverted to PWM
(c) grn: High-gate (*HG*) signal measured at pin4 of *LM2722*: synch to PWM

**(a)** LM27222.pin4: *IN* = PWM input




**(b)** LM27222.pin7: *LG* = *low-gate signal*




**(c)** LM27222.*pin2*: *HG* = *high-gate signal*

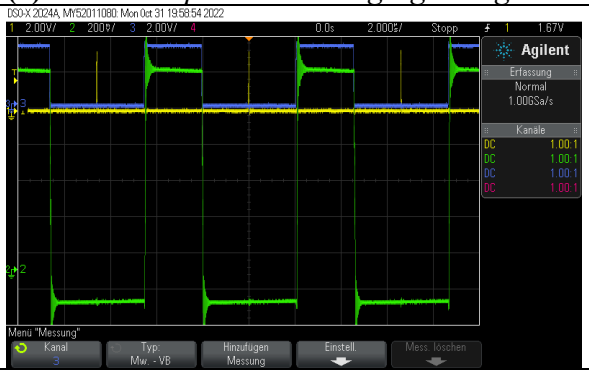



Fig. 2.3.1(a) illustrates, that the PWM signal coming from the *FPGA's* signal *pwmo* (blue) appears on as input on *pin4* = *IN* of the *LM27222*. Measure:

**IN = LM27222.pin4 low level = _____ , high level = _____ .**

Fig.2.3.1(b) illustrates, that the low-gate signal *LG* = pin7 is inverted to the PWM input when sw(1) = '1'; and *LG* = '0' otherwise.

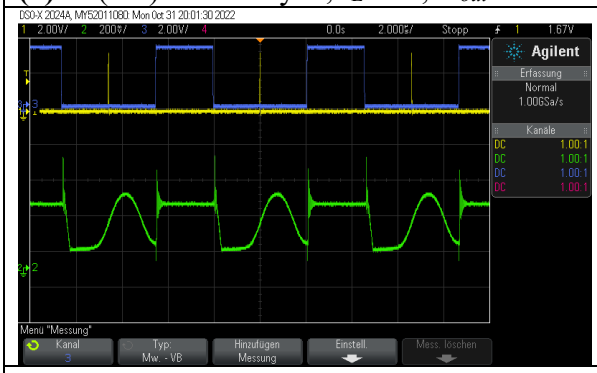
**LG = LM27222.pin7 low level = _____ , high level = _____ .**

Fig.2.3.1(c) illustrates, that the high-gate signal *HG* = pin2 is in phase with the PWM input signal, but has a strongly amplified *High* level.

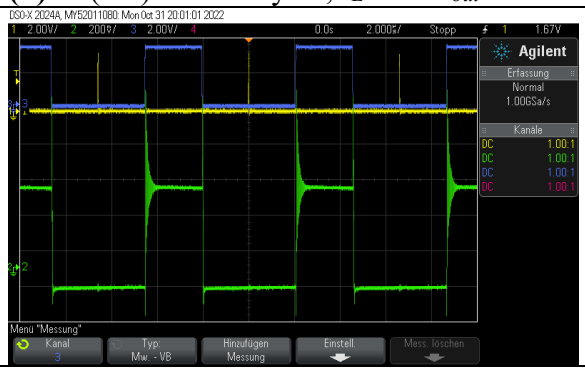
**HG = LM27222.pin2 low level = _____ , high level = _____ .**

## 2.3.2 Check Behavior of Switching Node *SW*

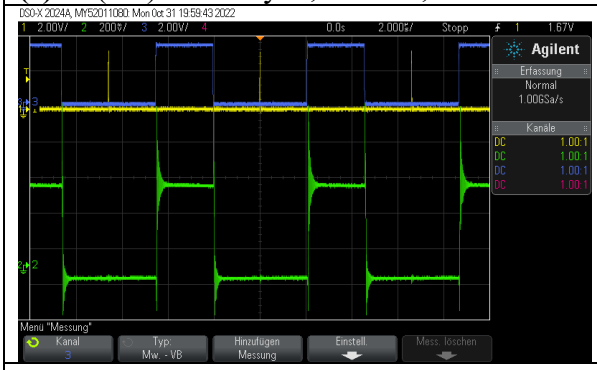
**(a)** *sw*(1:0)="00": async, $I_L$=0A, $U_{out}$=2.61V



**(b)** *sw*(1:0)="01": async., $I_L$=1A $U_{out}$=0.98V



**(c)** *sw*(1:0)="10": sync, $I_L$ = 0A, $U_{out}$=1.34V



**(d)** *sw*(1:0)="11": sync, $I_L$ = 1A, $U_{out}$=1.13V

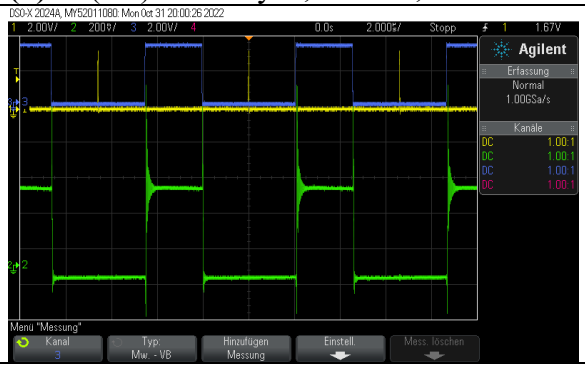


**Figure 2.3.2:** Behavior of switching node *SW* at constant pulse width for w=1250mV (*sw*(9:6)="0000"), constant due to (sw(5:4)="11"), switches setting: *sw*(9:0)="0000 11 00 xy"

In the following measurements, you may take $I_{out}$ and $U_{out}$ from the 7-segment display.

Fig. 2.3.2(a) shows voltage at switching node *SW* for async. operat. and $I_L$=0. Measure levels:

**(a) SW = low = ____ , high = ____ , $I_{out}$ = ____ , $U_{out}$ = ____ .**

Fig. 2.3.2(b) shows voltage at switching node *SW* for async. oper. and $I_L$=1A. Measure levels:

**(b) SW = low = ____ , high = ____ , $I_{out}$ = ____ , $U_{out}$ = ____ .**

Fig. 2.3.2(d) shows voltage at switching node *SW* for sync. oper. and $I_L$=0A. Measure levels:

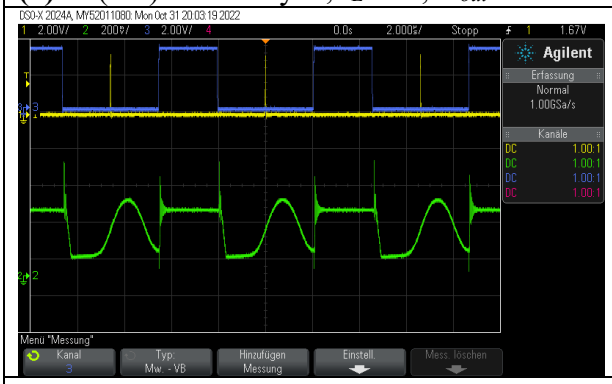
**(c) SW = low = ____ , high = ____ , $I_{out}$ = ____ , $U_{out}$ = ____ .**

Fig. 2.3.2(d) shows voltage at switching node *SW* for sync. oper. and $I_L$=1A. Measure levels:

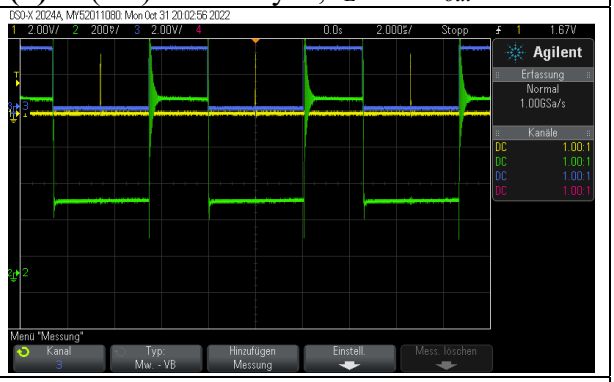
**(d) SW = low = ____ , high = ____ , $I_{out}$ = ____ , $U_{out}$ = ____ .**

## 2.3.3 Check Behavior of Bootstrap Node *CB*

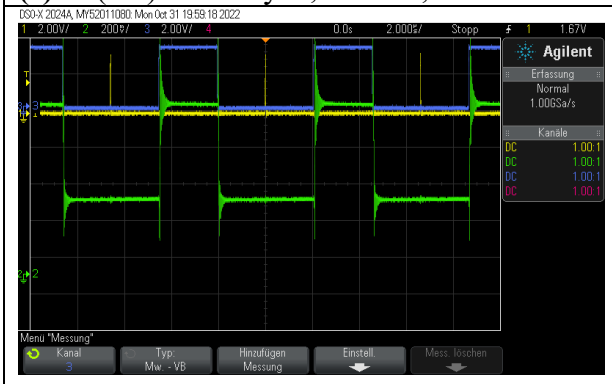
**(a)** *sw*(1:0)="00": async, $I_L$=0A, $U_{out}$=2.61V



**(b)** *sw*(1:0)="01": async, $I_L$=1A $U_{out}$=0.98V



**(c)** *sw*(1:0)="10": sync, $I_L$ = 0A, $U_{out}$=1.34V



**(d)** *sw*(1:0)="11": sync, $I_L$ = 1A, $U_{out}$=1.13V

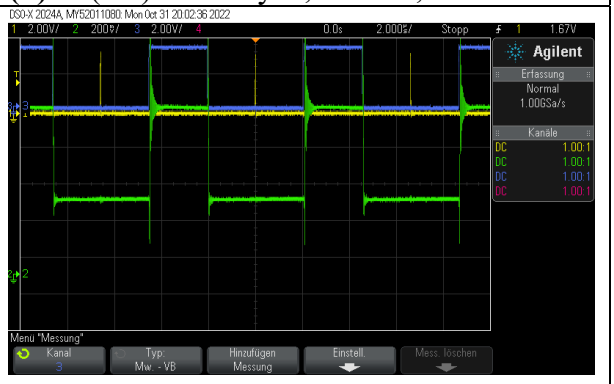


**Figure 2.3.3:** Behavior of bootstrap node *CB* at constant pulse width set for $U_{out}$=1250mV (by *sw*(9:6)="0000") at $U_{in}$ =3.3V, pulse-width is constant due to (sw(5:4)="11"), total switches setting is: *sw*(9:0)="0000 11 00 xy"

In the following measurements, you may take $I_{out}$ and $U_{out}$ from the 7-segment display.

Fig. 2.3.2(a) shows voltage at bootstrap node *CB* for async. operat. & $I_L$=0. Measure levels:

**(a) CB = low = ____ , high = ____ , $I_{out}$ = ____ , $U_{out}$ = ____ .**

Fig. 2.3.2(b) shows voltage at bootstrap node *CB* for async. operat. & $I_L$=1A. Measure levels:

**(b) CB = low = ____ , high = ____ , $I_{out}$ = ____ , $U_{out}$ = ____ .**

Fig. 2.3.2(c) shows voltage at bootstrap node *CB* for sync. operat. & $I_L$=0. Measure levels:

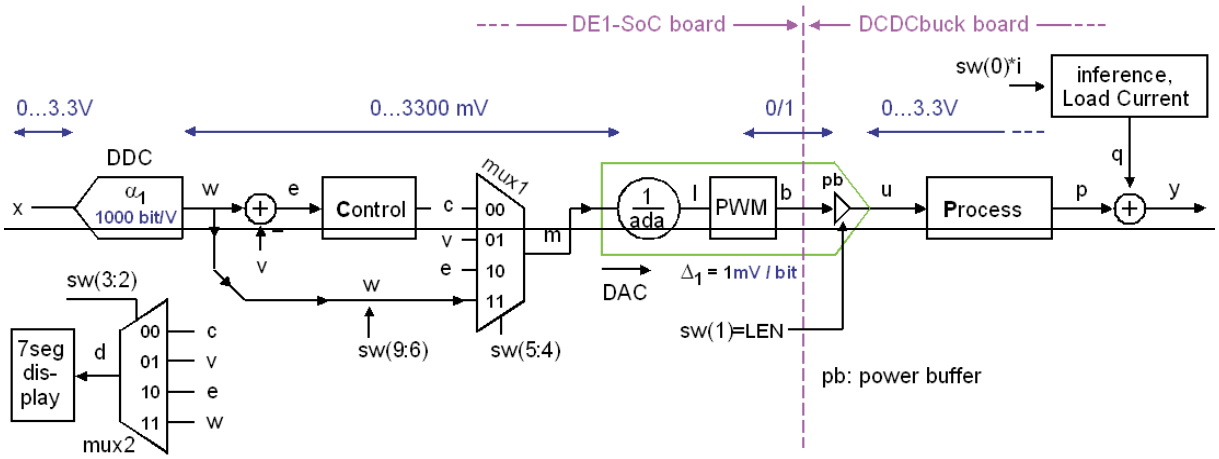
**(c) CB = low = ____ , high = ____ , $I_{out}$ = ____ , $U_{out}$ = ____ .**

Fig. 2.3.2(d) shows voltage at bootstrap node *CB* for sync. operat. & $I_L$=1A Measure levels:

**(d) CB = low = ____ , high = ____ , $I_{out}$ = ____ , $U_{out}$ = ____ .**

## 2.3.4 Computing DC Resistor $R_D$

**(a)** System setup




**(b)** *RLC* low-pass forming the process

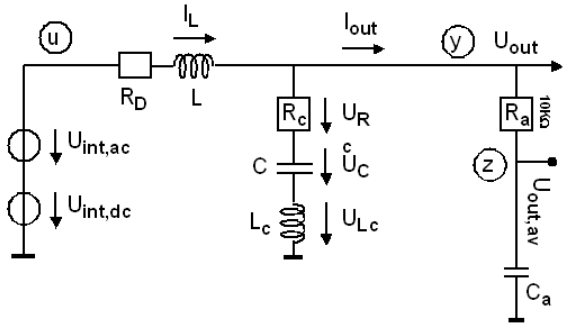



**Fig. 2.3.4:**
**(a) System setup,**
**(b)** Assuming the *RLC* lowpass to be driven by an inner DC source $U_{int.dc}$ and an serial AC source $U_{int.av}$.

According to Fig. 2.3.4 we model the PWM driver as DC source $U_{int.dc}$ plus AC source $U_{int.ac}$. The effect of the AC source is largely eliminated by the *RLC* low-pass filter, so that we can measure $U_{int.dc}$ as average output voltage at zero load current. After switching on the load current $I_{out}$, the average output voltage $U_{out.av}$ decreases by $R_D \cdot I_{out}$.

Set *sw* = "0000 11 00 10" to get *w*=1250mV, fixed pulse-width and synchronous operation.

Measure at sw(0)='0' : $U_{int,dc} = U_{out,av,OFF} =$ _____ mV, $I_{out,OFF} =$ _____ mA,

Measure sw(0)='1' : $U_{out,av,ON} =$ _____ mV, $I_{out,ON} =$ _____ mA,

Compute $R_D$(w=1250mV) = $\dfrac{U_{int,DC} - U_{out,av}}{I_{out,ON} - I_{out,OFF}} =$ _____ .

Hint: $R_D$ should be in the range of 140…160 mΩ.

Measured on board # 06 of type DCDCbuckRev10.02 on 18.11.2022
Measure at sw(0)='0' : $U_{int,dc} = U_{out,av,OFF} =$ 1332 mV, $I_{out,OFF} =$ 10 mA,
Measure sw(0)='1' : $U_{out,av,ON} =$ 1194 mV, $I_{out,ON} =$ 970 mA,
Compute $R_D$(w=1250mV) = (1332-1194)/(970-10)=0,144

### 2.3.5 Check Behavior for Zero Load Current

Try to explain the voltage bump of node *SW* when the high-side power *FET* is *OFF* in Fig. 2.3.2(a).

Despite *sw*(0)='0', a small load current flows. Repeat the measurement of Fig. 2.3.2(a) (with still bypassed controller: sw(5:4)="00") and remove Jumper *JP_Load*. What happens? Why?

Switch on the control unit: sw(5:4)="00". Switch sw(1) = synchronous mode briefly ON and OFF again. Observe $U_{out}$ and $U(SW)$. What happens? Explain!

Solutions to chapter 2.3.4:

Try to explain the voltage bump of node *SW* when the high-side power *FET* is *OFF* in Fig. 2.3.2(a).

1. **Low phase: In the first moment, when the high-side switch goes to OFF, the current through the coil is still flowing forward (into capacitor C) holding node SW down.**
2. **Positive ramp: After a while, the charge flows back from C through L to node SW, so that its node voltage rises.**
3. **Negative ramp: A small load current is still flowing, with muust be delivered through the coil pulling down again U(SW).**

Despite *sw*(0)='0', a small load current flows. Repeat the measurement of Fig. 2.3.2(a) (with still bypassed controller: sw(5:4)="00") and remove Jumper *JP_Load*. What happens? Why?

**$I_{out}$ = 0 now. Nodes *SW* and $U_{out}$ float up to higher voltages. *PWM* input pulses are still observed, but no more on nodes *SW* and *CB* -> the charge pump is dead.**

Switch on the control unit: sw(5:4)="00". Switch sw(1) = synchronous mode briefly ON and OFF again. Observe $U_{out}$ and *U*(*SW*). What happens? Explain!

**Same as above, but no more input pulses coming from *pwmo* are observed, because now the controller seeks to pull $U_{out}$ down.**

# 3 References


[1] *Texas Instruments*, "*LM27222 High-Speed 4.5A Synchronous MOSFET Driver*", avail.: https://www.ti.com/lit/ds/symlink/lm27222.pdf?ts=1662800602460&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FLM27222.

[2] *Linear Technology (today: Analog Devices)*, "*Low Noise, 500ksps, 8-Channel, 12-Bit ADC*", available: https://www.analog.com/media/en/technical-documentation/data-sheets/2308fc.pdf

[3] *Texas Instruments*, "*INA240 – 4-V to 80-V, Bidirectional, Ultra-Precise Current Sense Amplifier With Enhanced PWM Rejection*", available: https://www.ti.com/lit/ds/symlink/ina240.pdf?ts=1662820015241&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FINA240

[4] *Texas Instruments*, "*REF50xx – Low-Noise, Very Low Drift, Precision Voltage Reference*", available: https://www.ti.com/lit/ds/symlink/ina240.pdf?ts=1662820015241&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FINA240