Characterizing Passive Components of a DC/DC Buck Converter

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Practical Training using Board *DCDCbuck_Rev12*

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Abstract. The passive component RLC lowpass part of a DC/DC buck converter is characterized for understanding physical backgrounds, modeling and optimal control setting.

1 Introduction

1.1 Objectives

Goal of this practical training is the passive component characterization of a mixed analog/digital system using the example of a DC/DC buck converter with a digital control unit.

1.2 The *DCDCbuck* Daughter Board Hardware

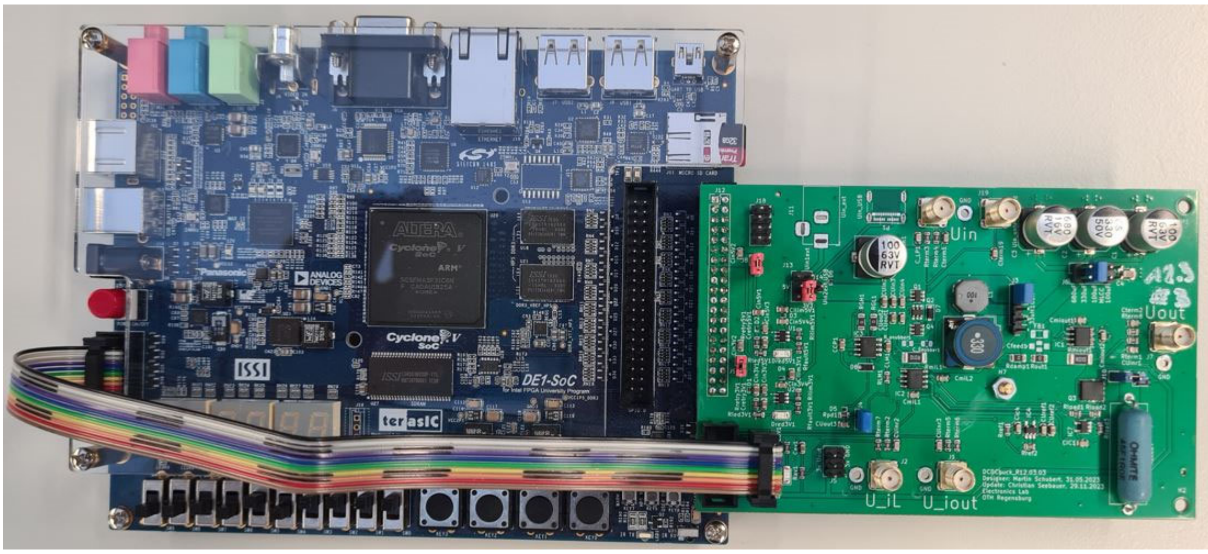


Fig. 1.1: *DE1-SoC* board (left) with plugged-in *DCDCbuck_R12.03* daughter board (right).

Fig. 1.1 shows the *DE1-SoC* board from Terasic [1-8] with *DCDCbuck_Rev10.02.06* daughter board fabricated by Florian Schwankner [10] in the Electronics Laboratory. The ribbon cable connects the input of the *DE1-SoC* on-board's *LTC2308* ADC [15] with output pins of the *DCDCbuck* boar

(a) Board photo, jumpers: red: power, blu: settings, grn: optional

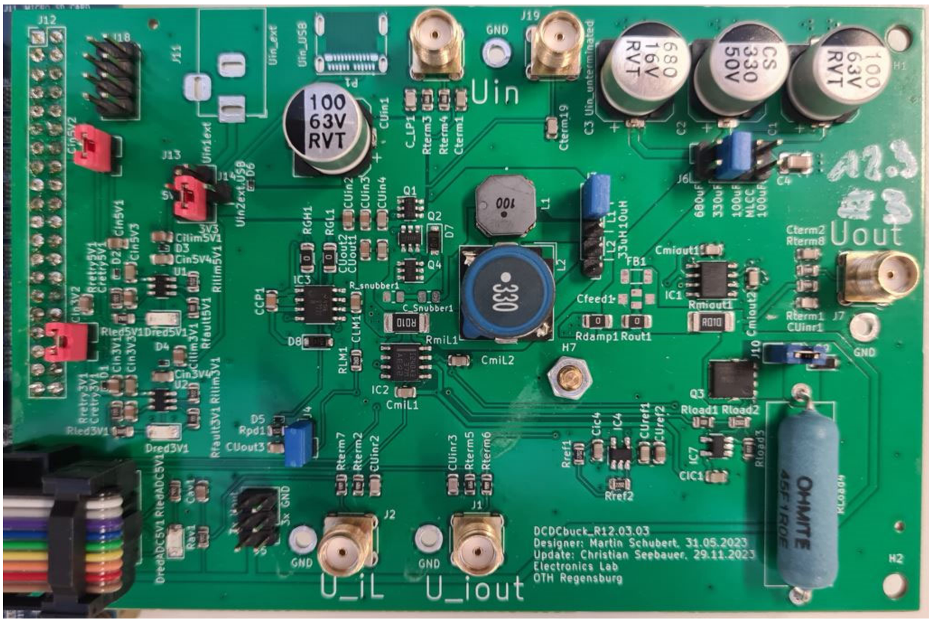


Fig. 1.2: daughter board *DCDCbuck Rev12.03.03*

Bord numbering scheme: *Rxx.yy.zz*, with
xx: Design/Designer, *yy*: No. of fabricated board, *zz*: No. of schematics update of design yy.

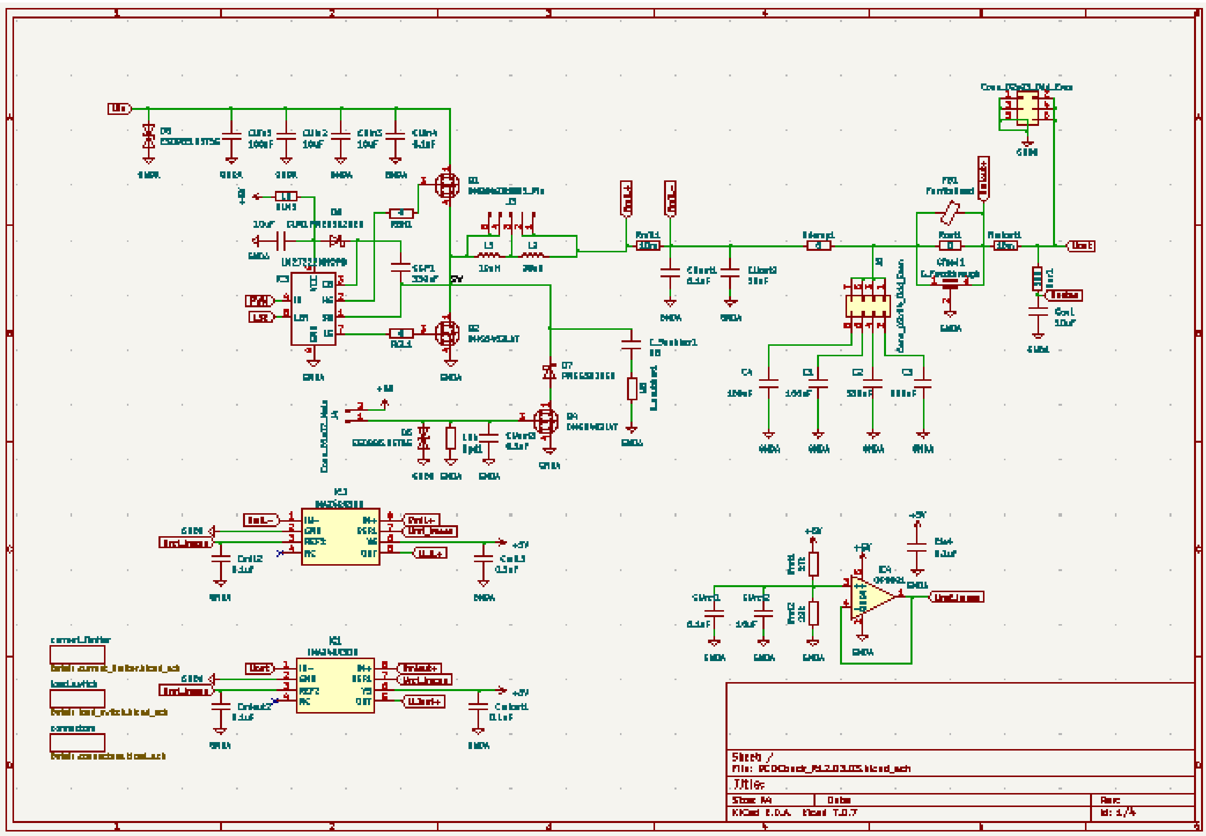
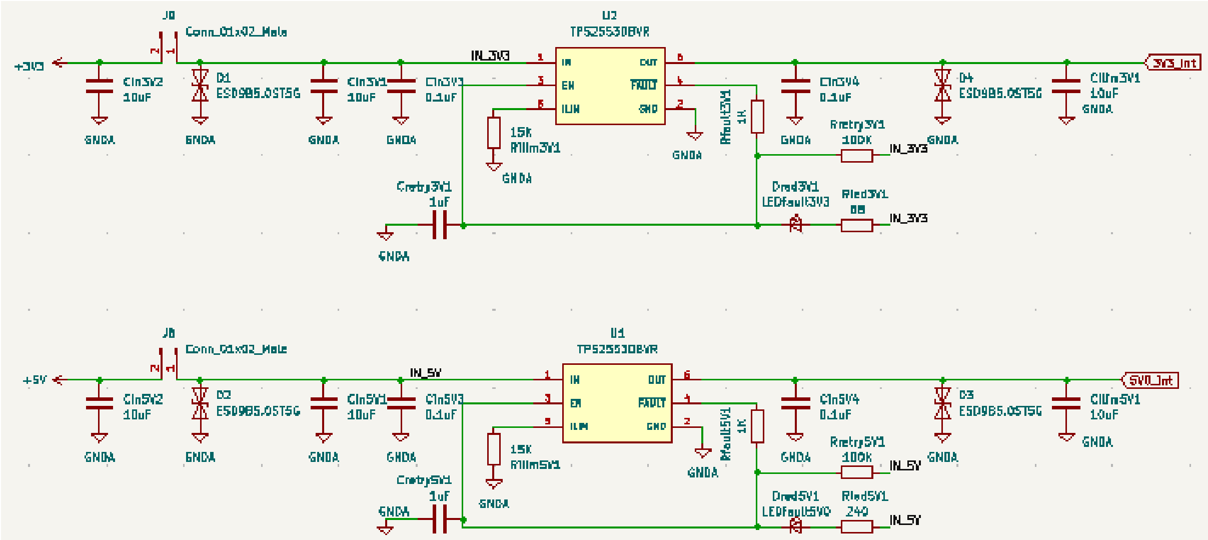
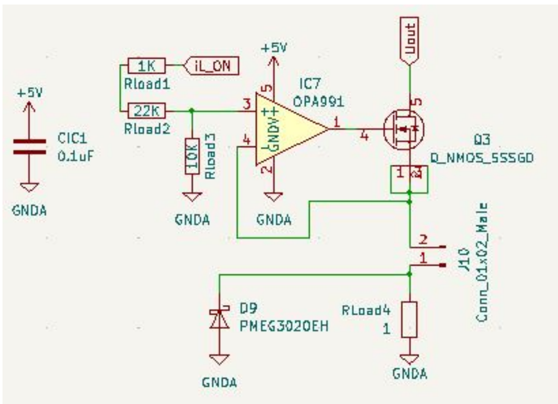


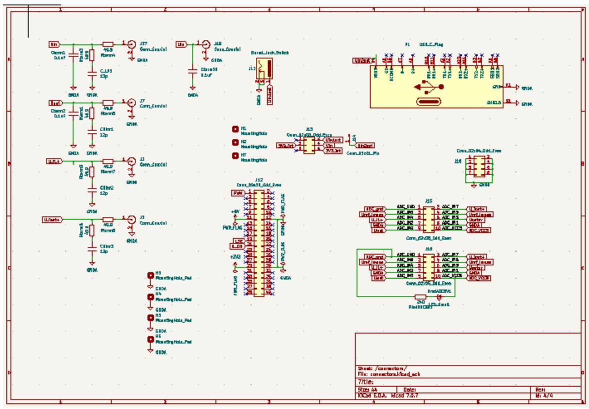
Fig. 1.3(a): *DCDCbuck_R12.03* board top level schematics (in *KiCad* software [19])



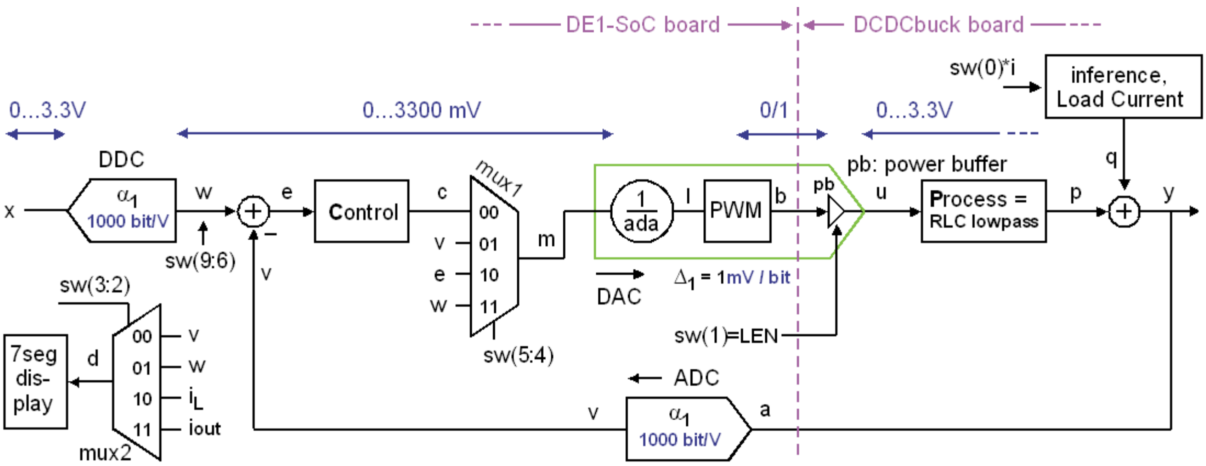
(b): *DCDCbuck_R12.03* board, subcircuit power supplies



(c) Subcircuit 1A Load Current



(d) Subcircuit Connectors



(e) Principal schematics of the DCDCbuck_R12.03 daughter board

Fig. 1.3: *DCDCbuck_R12.03* board, main circuit and subcircuits

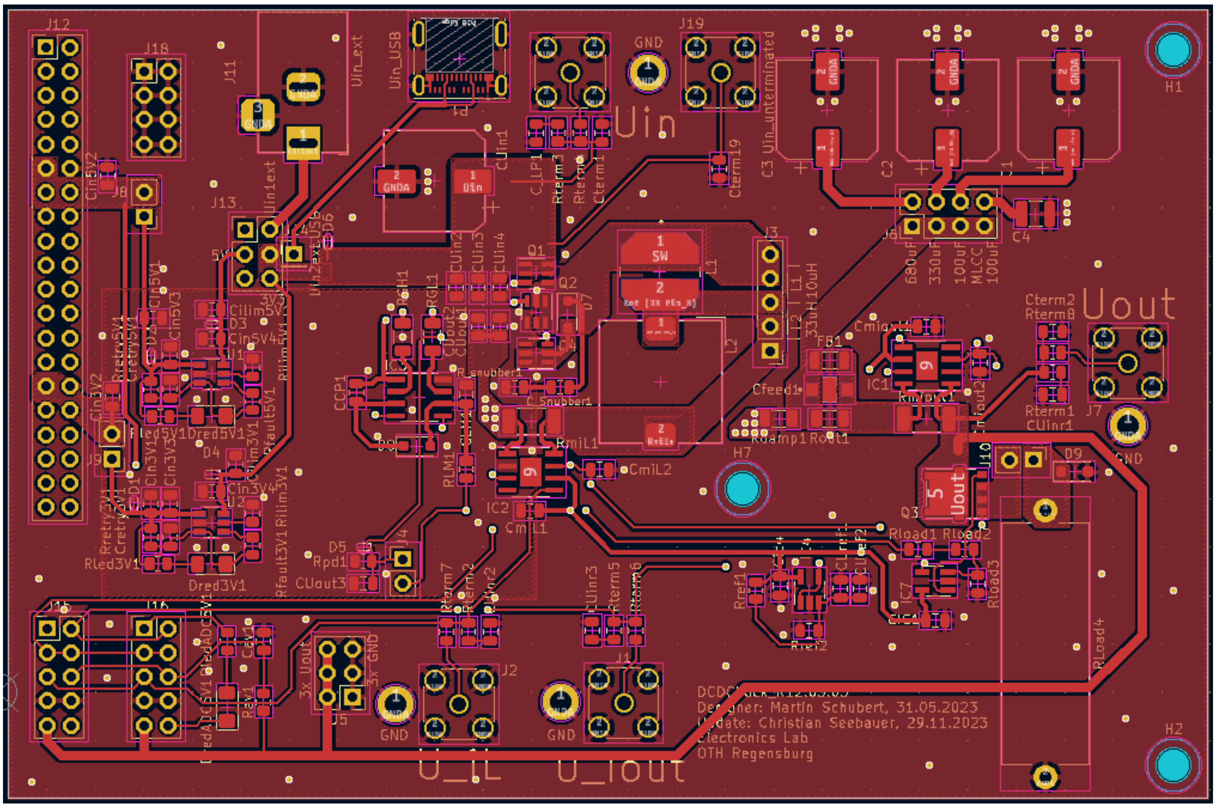


Fig. 1.4(a): *DCDCbuck_R12.03* front-side copper layer (*KiCad* [19])

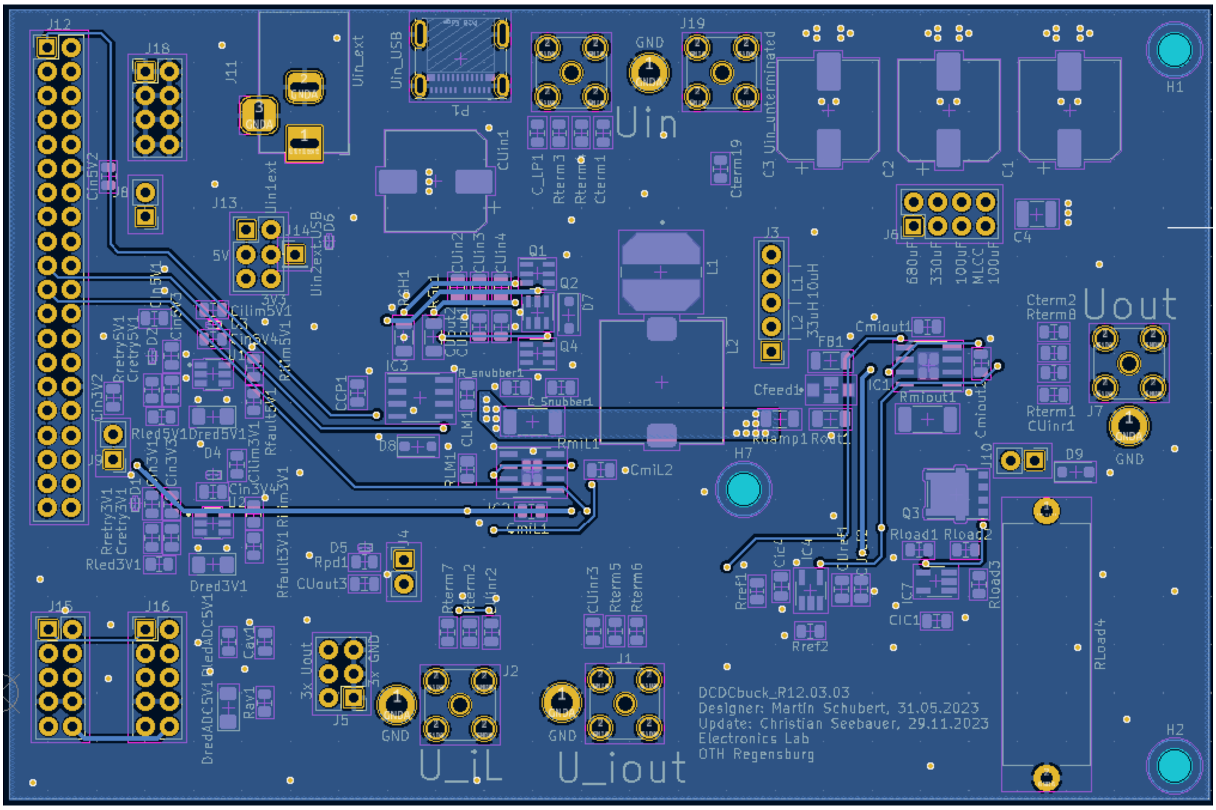


Fig. 1.4(b): *DCDCbuck_R12.03* back-side copper layer (*KiCad* [19])

Fig. 1.4 illustrates the layout (a) and photo (b) of the *DCDCbuck_Rev12.03.03* board. Vias connect different metal layers and may hold pins of plugs.

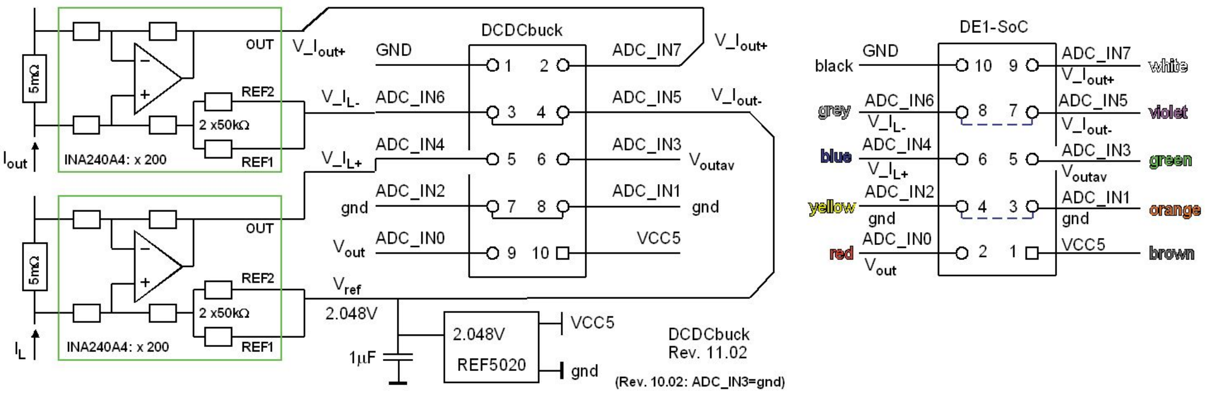


Fig. 1.5: Pin assignment of the 10-pin ADC input plug (connected by the 10 wire ribbon cable). It is a cross cable! Color code valid for $V_{CC}(ADC)$ = black. Numbers within the plug-box are the pin-numbers of the plug. Labels *ADC_IN#* (# = 1…8) indicate input channel number # of ADC *LTC2308* [15]. *ADC_IN3* is ground for board revisions *Rev* ≤ 11.01.

Fig. 1.5 illustrates the pin assignment of the 10-pin ADC input plug (connected by the 10 wire ribbon cable seen in the photo). Numbers within the plug-box are the pin-numbers of the plug. Label *ADC_IN#* (# = 1…8) indicates input channel number # of the ADC *LTC2308* [15]. *ADC_IN3* is ground for board revisions *Rev* ≤ 11.01.

1.3 Outline

The organization of this communication is as follows:

Section 1 introduces into this document.
Section 2 makes the student familiar with required tools.
Section 3 characterizes the passive *RLC* lowpass (labeled *Process* in Fig. 1.3) on the isolated *DCDCbuck* daughter board.
Section 4 draws conclusion and
Section 5 offers references.

2 Getting Started with the Tools

This chapter makes you familiar with some basic tools and formulae.

2.1 Fundamental Electronics

2.1.1 Inductor: Extract *L* and series wire resistor *R_w* from *Bode* Diagram

$X_L = sL \xrightarrow{s=j\omega} j\omega L$, consequently $L = \frac{|X_L|}{2\pi f}$

Inductor with serial wire resistor R_w:

$Z_{RL} = R_w + j\omega L$, consequently

$$L = \frac{\sqrt{|Z_{RL}^2| - R_w^2}}{2\pi f} \qquad (2.1)$$

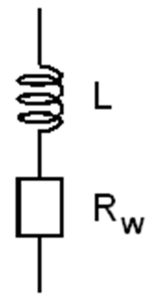


Fig. 2.1.2: *L, R* in series which models a real-world inductor. Example: Fig. 2.8.2.

If $R_w << |X_L|$ negligible: $L = \frac{\sqrt{|Z_{RL}^2| - R_w^2}}{2\pi f} \xrightarrow{|X_L| >> R_w} \frac{|Z_{RL}|}{2\pi f} = \frac{|X_L|}{2\pi f}$ (2.2)

PS: Data sheet note R_w as DC resistor, or *DCR*.

2.1.2 Capacitor: Extract *C* and series resistor *R_C* from *Bode* Diagram

$X_C = \frac{1}{sC} \xrightarrow{s=j\omega} \frac{1}{j\omega C}$, consequently $C = \frac{1}{2\pi f |X_C|}$

Capacitor with equivalent series resistor R_C:

$Z_{RC} = R_w + \frac{1}{j\omega C}$, consequently

$$C = \frac{1}{2\pi f \sqrt{|Z_{RC}^2| - R_C^2}} \qquad (2.3)$$

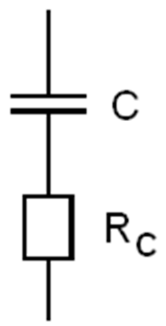


Fig. 2.1.2: *C, R* in series which models a real-world capacitor.

If $R_C << |X_C|$ negligible: $C = \frac{1}{2\pi f \sqrt{|Z_{RC}^2| - R_C^2}} \xrightarrow{|X_L| >> R_w} \frac{1}{2\pi f |Z_{RC}|} = \frac{1}{2\pi f |X_C|}$ (2.4)

PS: Data sheets label R_C as *equivalent series resistor*, or *ESR*.

2.1.3 Parallel LRC Oscillator: (*LR*||*C*: Real World Inductor)

Inductor with serial resistor *R* and parallel capacitor *C*:

$$Z_{LRC} = (R+sL) \| \frac{1}{sC} = \frac{R+sL}{1+sRC+s^2LC} \tag{2.5}$$

Using $s = j\omega$ delivers

$$Z_{LRC}(j\omega) = \frac{R+j\omega L}{1-\omega^2 LC + j\omega RC} \tag{2.6}$$

which peaks for small time constants *RC* near

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad \Leftrightarrow \quad f_0 = \frac{1}{2\pi\sqrt{LC}}. \tag{2.7}$$

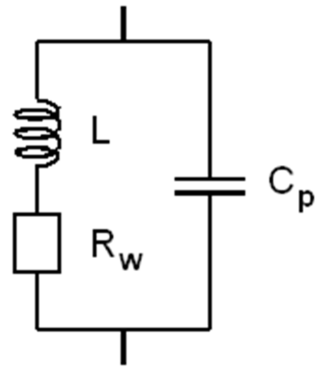


Fig. 2.1.3: LRC parallel, which models a real-world inductor. Example: Fig. 2.8.3 peak up (right).

2.1.4 Series *RLC* Oscillator (Real-World Capacitor)

In series with the capacitor and its resistor R_C we have a series inductor *L*

$$Z_{CRL}(s) = R + sL + \frac{1}{sC} = R_C + \frac{1+s^2LC}{sC} \tag{2.8}$$

and with $s = j\omega$

$$Z_{CRL}(\omega) = R - j\frac{1-\omega^2 LC}{\omega C}. \tag{2.9}$$

At $\omega_0 = \frac{1}{\sqrt{LC}} \quad \Leftrightarrow \quad f_0 = \frac{1}{2\pi\sqrt{LC}}$ we get

$$Z_{CRL}(f) \text{ is minimal} \tag{2.10}$$

and

$$Z_{CRL}(f_0) = R. \tag{2.11}$$

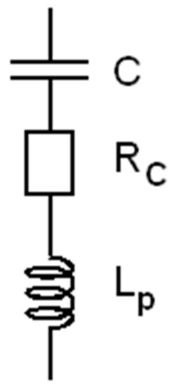
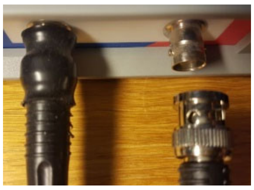


Fig. 2.1.4: LRC parallel oscillator, which models a real-world capacitor. Example: Fig. 2.8.3, peak down (left).

In summary, at the impedance minimum in the frequency domain we also have phase 0. At this point we can read the series resistor (i.e. R_C of a capacitor) and the resonant frequency f_0.

2.2 Basic Metering

(a) *BNC* plugs



(b) *BNC* ⇔ banana adaptor

(c) BNC 50Ω

(d) BNC ⇔ pin plugs

(e) multimeter, adaptor and 50Ω

Fig. 2.2: Different *BNC* related measurements aids

Most measurements are based on *BNC* and pin cables and plugs as illustrated in Fig. 2.1.

2.3 *KiCad* Layout and Schematic Editor

Download the DCDC converter schematics from the author's homepage > [Schubert.OTH] >…*Edu* > *Labs* > *labs with DE1-SoC Board and Daughte Boards* > *Models_ADA+DCDCbuck_edu_R10_&12.zip* > unzip > Layout+Schematic > Layout_DCDCbuck_Rev12.03.03_Seebauer.upd_2024s.zip > unzip > DCDCbuck_R12.03.03_Seebauer.upd_ordered_2024s*.*brd*: physical board layout

- *.*pro*: project file, from there open ->
- *.*sch*: board schematic
- *.*pcb*: board layout

2.4 *HM8118 LCR* Bridge for Device Characterization

LCR bridge *HM8118* [HM8118] is available in the electronics lab and suitable to measure components such as capacitors and inductors. Check for the *HM8118 LCR* bridge in the lab and measure some arbitrary inductors and capacitors.

Note that we measure series resistors only, so the *MODE* button must be *AUTO* and/or *SER*. Typically it is enough to press *AUTO* and let the *HM8118* detect the rest.

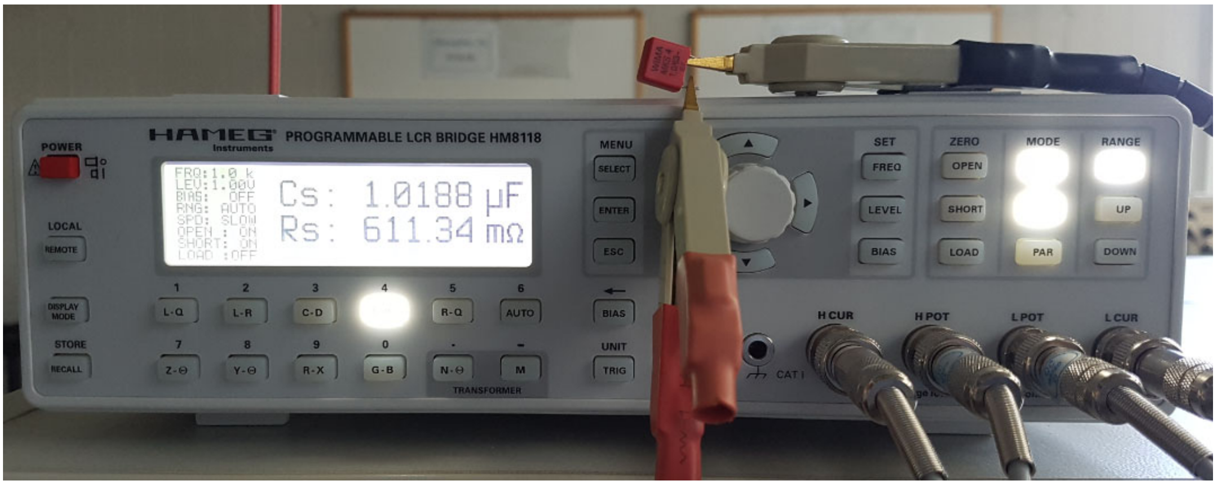


Fig. 2.4: Measuring a capacitor and its equivalent series resistor with HM8118

2.5 Screen Copies with *Microsoft Windows 10*

Screen copies with *MS Windows 10* can be made with the snipping tool: Start menu: → hit keys "*sn*" → (Snipping tool opens)→ *New* → (draw the widow to copy) → *File* → *Save as* → (filename). From the authors experience *Snipping* tool screen copies make smallest file sizes with *PNG* formatted files

2.6 Waveform Generator (*DSO-X 2024A*)

Use the waveform generator within oscilloscope *DSO-X 2024* [*DSO-X 2024A*] if available.

Observe generated waveforms by connecting *GEN OUT* with input channel 1 (*CH1*).

Measure the output impedance of your waveform generator. For more background information on this measurement see [I/O-Imp] at the author's homepage > *Offered Education* > *Lessons* > *Characterization* > *Considering I/O Impedances*.

- Create any waveform or a DC voltage with the waveform generator. Note the unloaded output voltage as U_{Gint}, which is measured as U_{Gext} with no load, i.e. $R_L \rightarrow \infty$, in Tab. 2.6.
- Load the source with a load resistor R_L, which should be of similar size as the output impedance to be measured, i.e. for typical waveform generators $R_L \sim 50\Omega$. Use an Ohm-meter to determine R_L exactly. Note the results in table 2.6.
- Measure U_{Gext} with load resistor and compute $\alpha = U_{Gext} / U_{Gint}$.
- Compute R_G from $R_G = \frac{1-\alpha}{\alpha} R_L$.

Table 2.6: Computing output impedance of waveform generator

Bench # 00	ideal	real	|	formula	ideal	real
U_{Gint}	2 V		|	xxx	xxx	xxx
U_{Gext}	1 V		|	$\alpha = \frac{U_{Gext}}{U_{Gint}}$	0.5	
R_L	50 Ω		|	$R_G = \frac{1-\alpha}{\alpha} R_L$	50 Ω	

Listing 2.6: Matlab code computing the generator's output resistor R_G.

```
% Computing an output Resistor
UGint = 1;
UGext = 499e-3;
RL    = 50.3;
alpha = UGext / UGint;
RG    = RL*(1-alpha)/alpha;
```

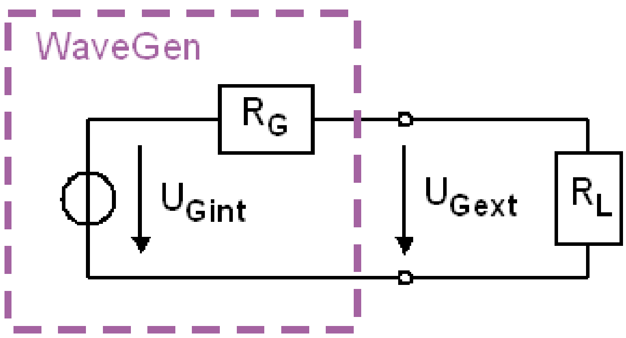


Fig. 2.6: Waveform generator with inner resistor R_G, external load resistor R_L, assumed inner generator voltage U_{Gint} and measured external voltage U_{Gext}.

2.7 Oscilloscope (*DSO-X 2024A*)

Use the waveform generator within oscilloscope.

- Generate a sinusoidal waveform and observe it with channel 1 (CH1) of your oscilloscope.
- Feed the same signal over a shunt resistor of R_S = 1 MΩ to channel 2 (CH2) as illustrated in Fig. 2.7.
- Measure the voltage drop of CH2 versus CH1 at low frequencies. To avoid the measurement of noise, it might be the best to measure the *RMS value of N cycles* with the oscilloscope. The voltage drop should be some 50%, e.g. from 2V → 1V.
- Increase frequency until you observe further -3dB (i.e. factor $1/\sqrt{2}$) decrease compared to DC-amplitudes, measured at 10Hz, e.g. from 1V → 0.71V

Table 2.7: Computing input impedance of waveform generator

Bench #	ideal	real	|	formula	ideal	real
$U_{Ch1}(f)$	2 V		|	$R_{in} = \frac{\alpha}{1-\alpha} R_S$	1 MΩ	
R_S	1 MΩ		|	$R_p = R_S \parallel R_{in}$	500 KΩ	
$U_{Ch2}(10Hz)$	1 V		|	$f_p = f\left(\frac{U_{Ch2,DC}}{\sqrt{2}}\right)$	29 KHz	
$\alpha = \frac{U_{Ch2}(10Hz)}{U_{Ch1}}$	½		|	$C_{in} = \frac{1}{2\pi f_p R_p}$	11 pF	

Listing 2.7: *Matlab* code computing R_{in}+C_{in}.

```
% Compute parallel RC input impedance
% at (*) insert your measured value
Uch1       = 703e-3;          % (*)
Uch2_10Hz  = 349e-3;          % (*)
alpha      = Uch2_10Hz/Uch1;
RS   = 1.01e6;                % (*)
Rin  = RS*alpha/(1-alpha);
Rp   = RS*Rin/(RS+Rin);
fp   = 29000;                 % (*)
Cin  = 1/(2*pi*Rp*fp);
Cin_datasheet = 11.0e-12;
```

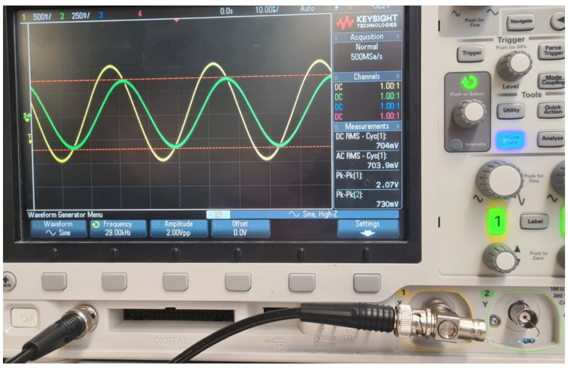
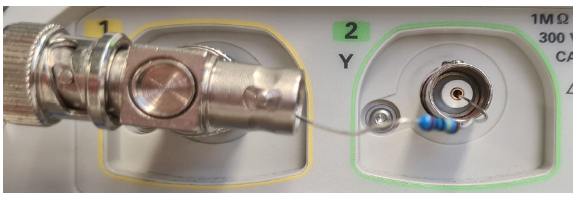


Fig. 2.7: *CH1* is directly connected to the 50Ω signal source, *CH2* is connected via a 1MΩ resistor.



2.8 *Bode* Diagram Measurements Using *Bode100*

2.8.1 Transfer Function Measurements

This chapter helps you getting started with using the *Bode100* [Omicron] instrument and the *Bode Analyzer Suite* [Bode100] operating it. **At Bode100 hardware, do not remove the BNC cable connecting *OUTPUT* with *CH1* input unless you are explicitly asked to do so.**

Connect the *Bode100 OUTPUT* to oscilloscope *CH1* input. Let *Bode100* output 0 dB (e.g. at 1KHz). To what effective ("*rms*") voltage and peak-to-peak voltage does that correspond?

Bode100 OUTPUT = 0 dB correspond to: U_{rms}(0dB) = ... ⇔ U_{pp} = ...

What power will this output dissipate at a 50Ω load? (Consider the 50Ω output impedance.)

P_{out} = ...

Measure with *DSO-X 2024A* oscilloscope
- Press button: *Autoscale*
- *Meas > Add measurement > Source 1, Type: Peak – Peak*
- *Meas > Add measurement > Source 1, Type: AC RMS, N Cycles*

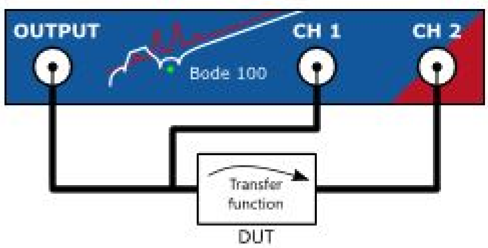
***Gain/Phase* measurement with *Bode100* (according to Fig. 2.8.1)**
- Use a short *BNC* cable to connect *OUTPUT* with *CH2* input.
- Start *Bode Analyze Suite* while *Bode100* being on and connected to your PC.
- Start a *Gain/Phase* measurement with default settings
- Shut down *Bode Analyze Suite* discarding changes.

Impedance Analysis* with *Bode100
- Plug a 50Ω BNC termination resistor onto the Bode100 output
- Restart *Bode Analyze Suite*, select *Impedance Analysis > Start Measurement* with default settings.
- Click into the *Bode* diagram and select *Optimize* with right mouse button.

Note: The File → Save [as] command of *Bode100* saves both setup and measured data.

Exercise: Perform a *One-Port Impedance Analysis* at any capacitor, as illustrated in Fig. 2.8.2. Compute the capacitance and its parasitic series inductance.

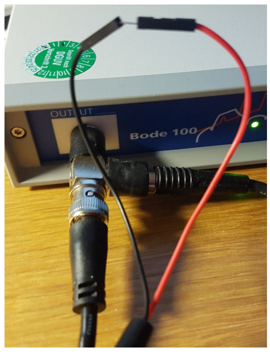
Fig. 2.8.1: Measure a *Bode* diagram with *Bode100* operated with *Bode Analyzer Suite 3* [Bode100], *Gain/Phase* Measurement.



2.8.2 OnePort Impedance Measurement: Cable BNC - pin

(a) Right: Photo of the measurement setup.

(b) Bottom: *One-Port Impedance* measurement with *Bode100*. We see a parasitic inductor at high frequencies.



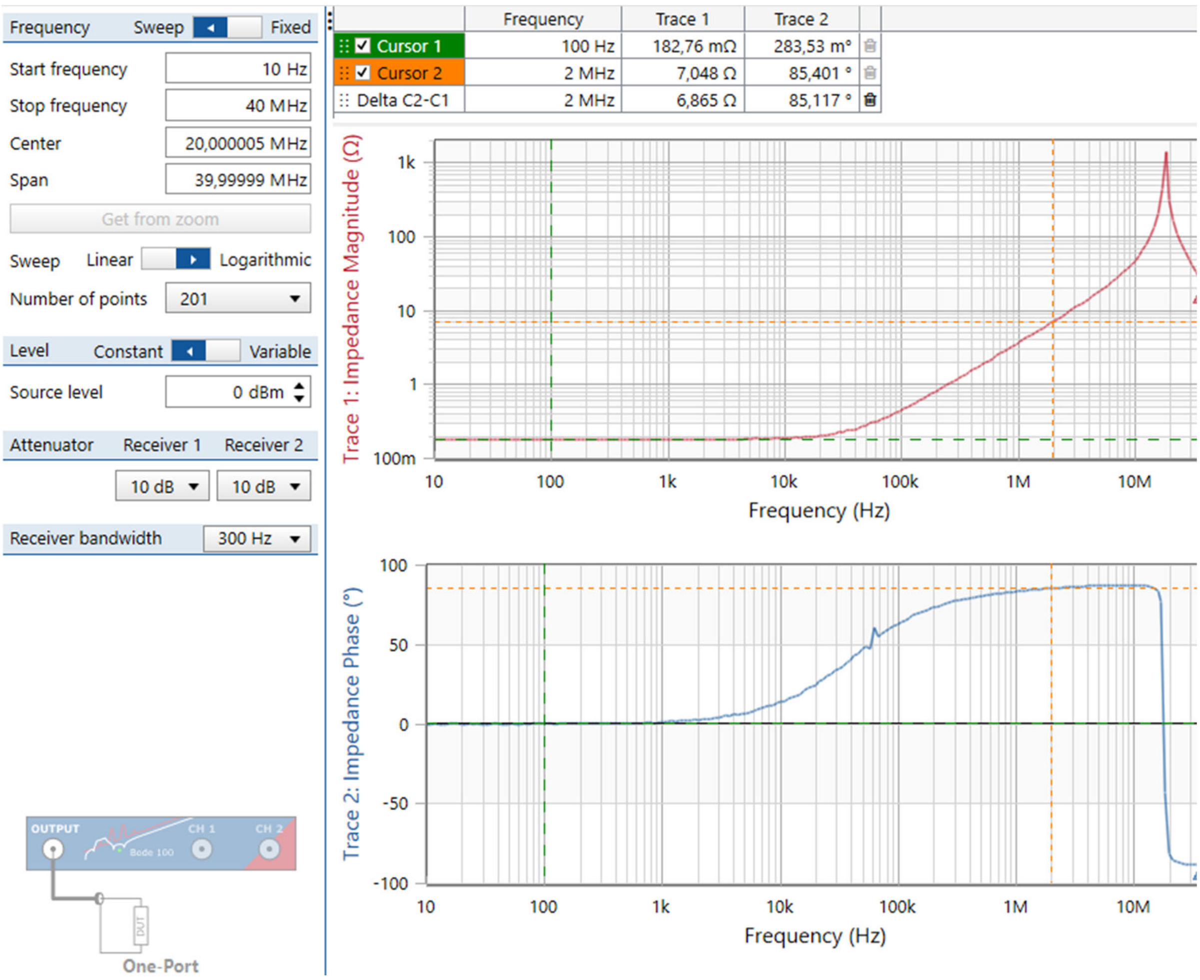


Fig. 2.8.2: *Bode100 One-Port Impedance* measurement of some mm of wire.

The *One-Port Impedance* measurements at straight logarithmic slopes delivers …

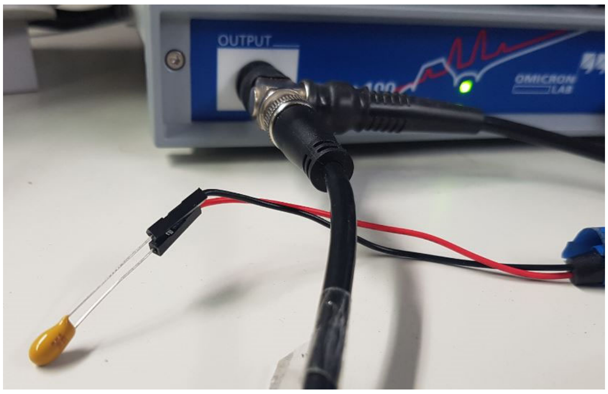
at f = 100Hz: ***R**cable* **=** . . . .

f = 2MHz: $X_L = R_w + j\omega L \rightarrow L = \frac{\sqrt{|X_L|^2 - R_w^2}}{2\pi f} =$ . . . . $\cong \frac{|X_L|}{2\pi f} =$ . . . .

2.8.3 OnePort Impedance Measurement: Capacitor BNC – pin

(a) Right: Photo of the measurement setup.

(b) Bottom: *One-Port Impedance* measurement with *Bode100*. We see a capacitor at low frequencies and a parasitic inductor at high frequencies.



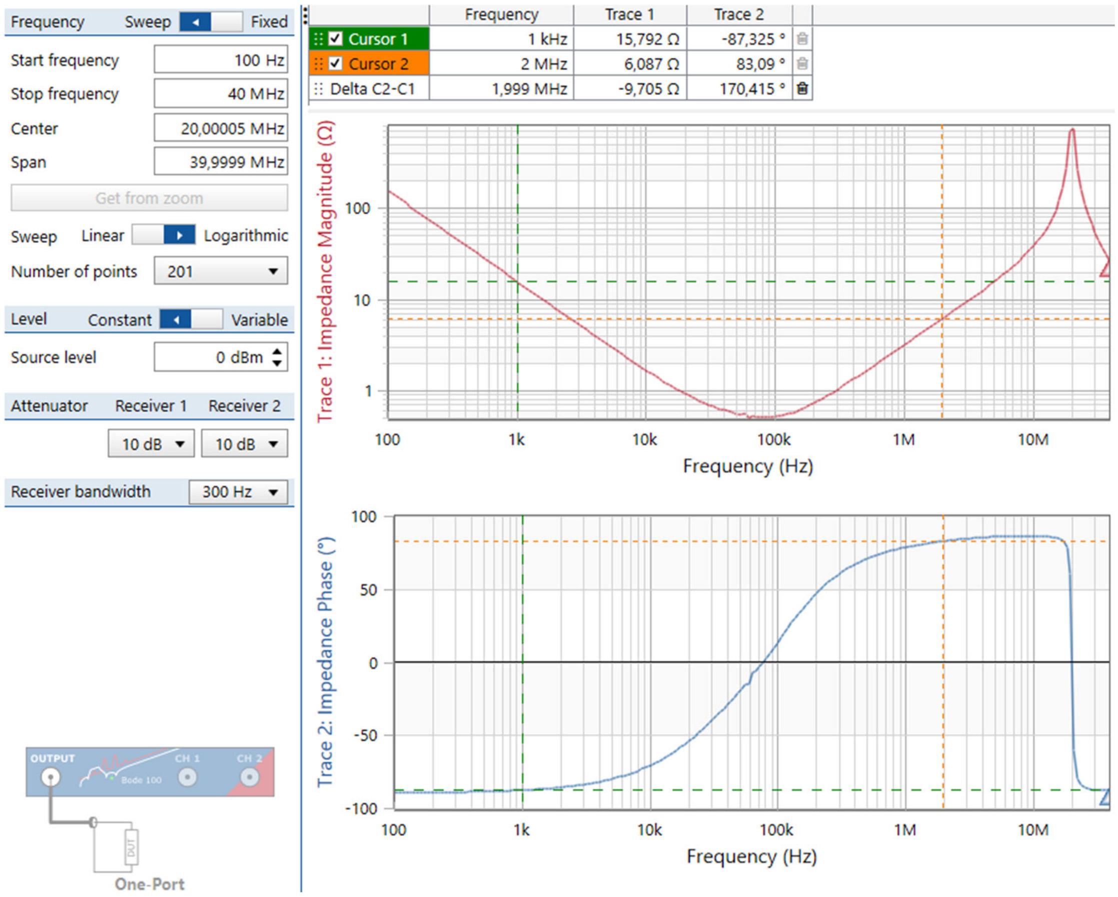


Fig. 2.8.3: *Bode100 One-Port Impedance* measurement of a capacitor of nominal 10 µF.

The *One-Port Impedance* measurements at straight logarithmic slopes delivers …

at f = 100Hz: $X_C \cong \dfrac{1}{j\omega C} \quad \rightarrow \quad C \cong \dfrac{1}{2\pi f\,|X_C|} \qquad =$

at f = 2MHz: $X_L \cong j\omega L \quad \rightarrow \quad L \cong \dfrac{|X_L|}{2\pi f} \qquad =$

How do you explain that inductor *L* is smaller now than above with the short only?

3 Passive *RLC* Lowpass on Isolated *DCDCbuck* Board

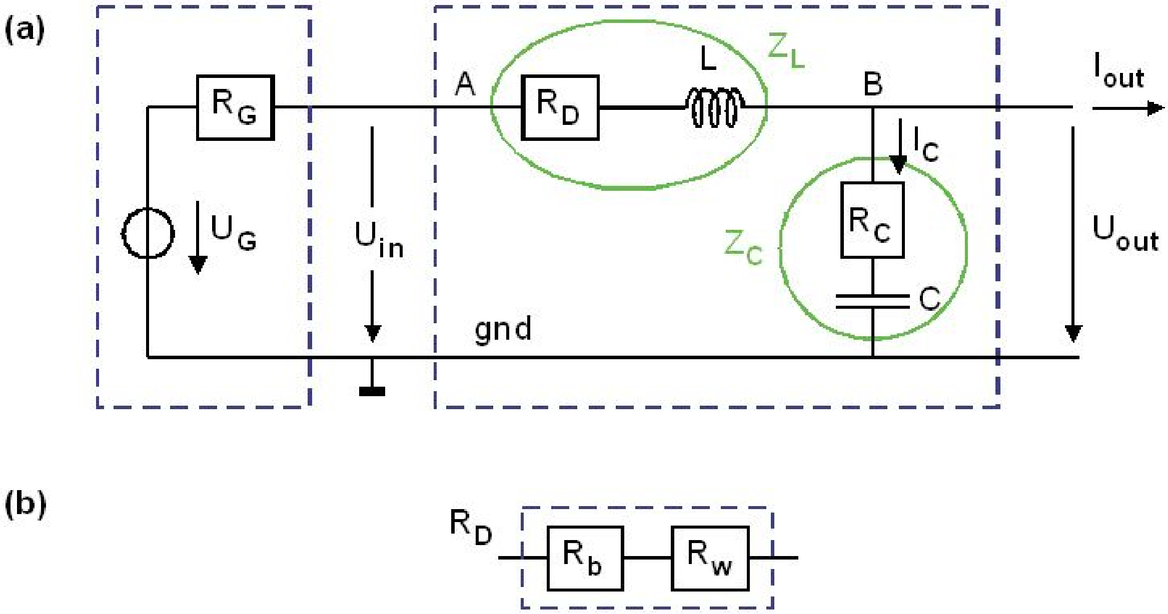


Fig. 3.0: *RLC* lowpass corresponding to boxes *Process* and *Inference* in Fig. 1.1

In this section the board is characterized isolated. Fig. 3.0 shows the *RLC* lowpass operated as demodulator of the pulse-width modulator (PWM). For 2nd order lowpass behavior, frequencies f higher than cut-off frequency f_0 will be attenuated according to $(f_0/f)^2$ corresponding to 40 dB/dec. As a rule of thumb, sampling frequency f_s should be $f_s \geq 10\ldots100\, f_0$, to yield a suppression of the PWM sampling frequency of $10^2\ldots10^4$ corresponding to 40…80 dB.

In our example we use the nominal values of $C = 100\mu$F, $L = 33\mu$H.

$f_s = f_{clock}$ / *pwm_period* = 50MHz / 330 =

. . . .

and $f_0 = \dfrac{1}{2\pi\sqrt{LC}} = \dfrac{1}{2\pi\sqrt{100\mu F \cdot 33\mu H}} =$

. . . .

The ratio f_s/f_0 is $\dfrac{f_s}{f_0} =$

. . . .

Consequently, a 3.3V_{pp} sinusoidal wave at f_s should be suppressed with a second order lowpass featuring a cut-off frequency f_o to . . . . mV_{pp}

…if the filter really was a second order lowpass only up to frequency f_s. However, is the attenuation f_0 really that big? When not, why? Let’s check these questions!

3.1 Output Capacitor Characterization

3.1.1 Main Capacitor Key Parameter measures with *HM8118*

Identify the 3 capacitors on the *DCDCbuck* board and characterize them. Use *LCR* Bridge *HM8118* in *OTH Regensburg's Electronics Lab* (see → Fig. 2.4) The capacitor's equivalent series resistor (*ESR*) is labeled R_C in Fig. 3.0.

Table 3.1.1: Capacitors

Board #	Capacitance maximum voltage 35V		Equivalent series resistor (ESR, R_C)		$R_C = \frac{1}{\omega_x C}$:	$f_x = \frac{1}{2\pi R_C C}$
	datasheet typical	measured µF	datasheet, typical	measured mΩ	Typical KHz	calculated KHz
C_1	100 µF		0.26 Ω		6.12	
C_2	330 µF		0.08 Ω		6.03	
C_3	680 µF		0.06 Ω		3.90	

The process transfer function's (PTF's) behavior shows additional effects for frequencies >10KHz. For better understanding we measure the output capacitor of nominal 680 µF in detail. Obviously, there is a serial build-in inductor in this capacitor.

Listing 3.1.1: *Matlab* computation of frequencies f_{xC} where $R_C=1/(\omega_x\, C)$

```
clear all;
% Computing the zeros of capacitors and series resistors
C_datasheet(1)  = 100e-6;  Rc_datasheet(1) = 260e-3;
C_datasheet(2)  = 330e-6;  Rc_datasheet(2) = 80e-3;
C_datasheet(3)  = 680e-6;  Rc_datasheet(3) = 60e-3;

C_measured(1) = 104.4e-6;  Rc_measured(1) = 146e-3;
C_measured(2) = 325.3e-6;  Rc_measured(2) = 83.5e-3;
C_measured(3) = 640.5e-6;  Rc_measured(3) = 68.3e-3;

% Computing the Poles
for i=1:3;
  fxC_datasheet(i) = 1 / (2*pi*Rc_datasheet(i)*C_datasheet(i));
  fxC_measured(i)  = 1 / (2*pi*Rc_measured(i)*C_measured(i));
end;
fxC_datasheet, fxC_measured
```

3.1.2 *Bode100* Measurement of the 100µF Output Capacitor Isolated

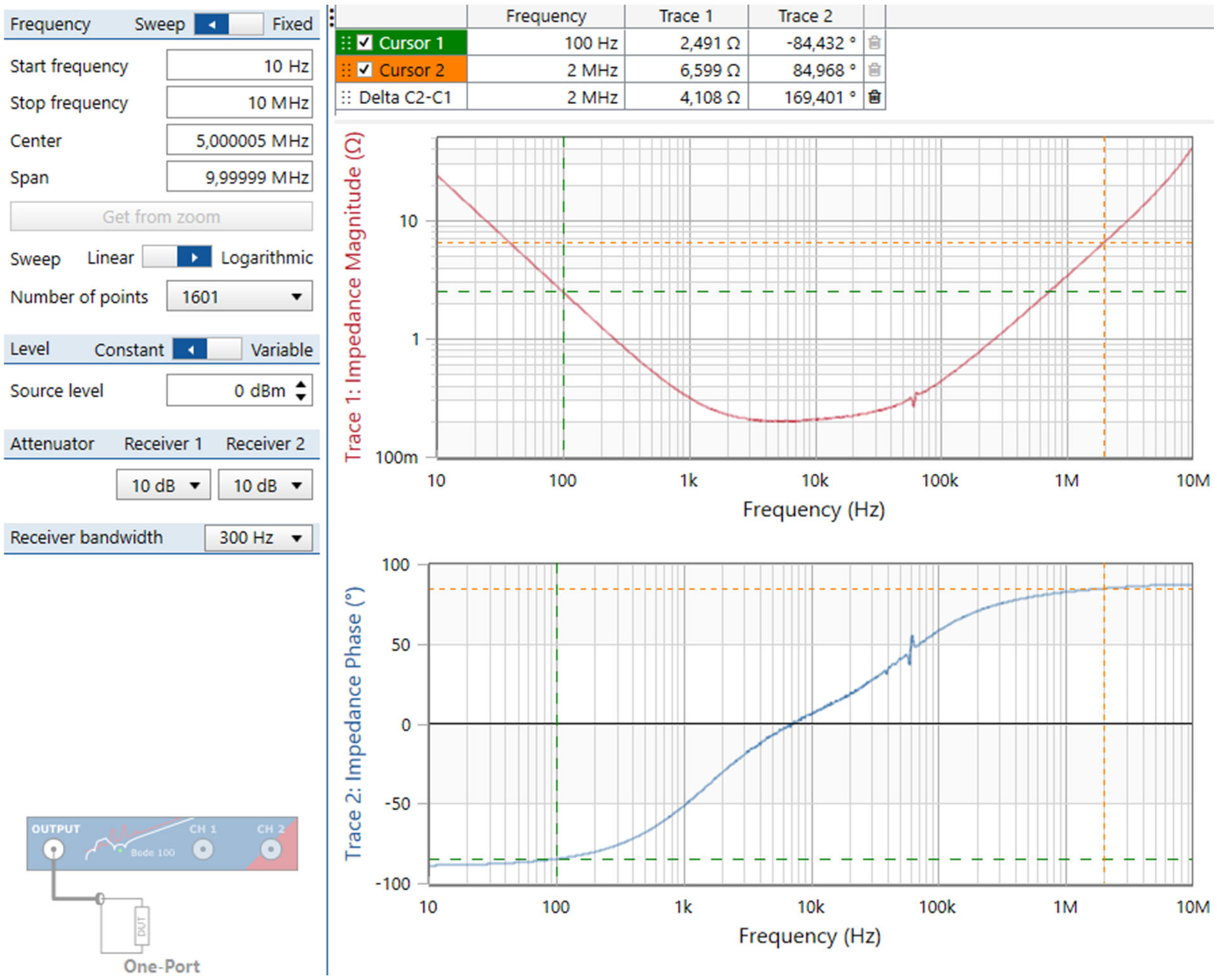


Fig. 3.1.2: *Bode100 One-Port Impedance* measurement of isolated 680µF (nominal) capacitor.

Bode100 One-Port Impedance measurements at straight logarithmic slopes deliver

at f = 100Hz: $X_C = \frac{1}{j\omega C} \rightarrow C_{C,680} = \frac{1}{2\pi f |X_C|} =$

. . . .

at f = 2MHz: $X_L = j\omega L \rightarrow L_C = \frac{|X_L|}{2\pi f} =$

. . . .

3.1.3 Measurement of the 100µF Output Capacitor Connected to Output

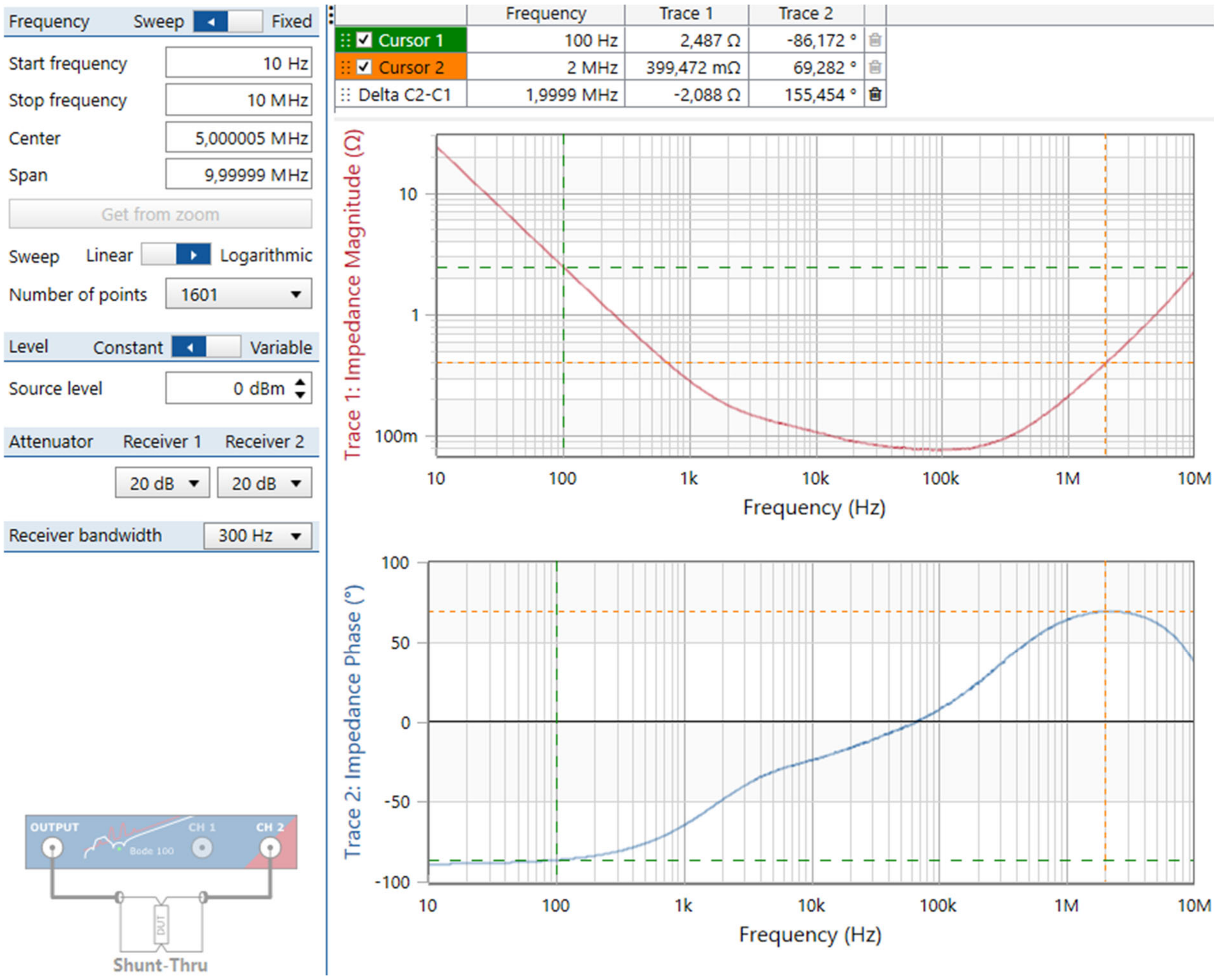


Fig. 3.1.3: *Bode100 Shunt-Thru Impedance* measurement of connected 680µF (nominal) capacitor connected to point *B* in Fig. 3.0.

Use a jumper to connect the 680µF-capacitor to the output node labeled *B* in Fig. 3.0. *Bode100 Shunt-Thru Impedance* measurements at straight logarithmic slopes deliver

at f = 100Hz: $X_C = \frac{1}{j\omega C} \rightarrow C_{B,680} = \frac{1}{2\pi f |X_C|} =$ ....

at f = 2MHz: $X_L = j\omega L \rightarrow L_B = \frac{|X_L|}{2\pi f} =$ ....

Winding capacitors to increase their capacitance creates a parasitic inductor.

3.2 Inductor Characterization

3.2.1 Measuring Inductor Parameters with *HM8118*

Identify the 2 inductors on the *DCDCbuck* board and characterize them. Use *HM8118* in OTH's Electronics Lab. Their DC resistor (DCR) is labeled wire-resistor R_w in this document. In Fig. 3.0, the total DC resistor $R_D = R_b + R_w$, whereas R_w inductors wire resistor and R_b the additional board resistor. R_D is the total resistor measured from point *A* to point *B* in Fig. 3.0.

Measure all inductors with *HM8118* and with disconnected capacitors.

Identify the 2 inductors on the *DCDCbuck* board and characterize them. Their DC resistor (*DCR*, labeled wire resistor R_w in this document) from the data sheet:

[Ref_L] Farnell, Coilcraft SMT Power Inductors – MSS1278T: available Jan. 2020: http://www.farnell.com/datasheets/1681957.pdf?_ga=2.267884619.41524489.1580808408-37263841.1580808408

Table 3.2.1: Inductors

Board #	Inductance		DC Resistance (*DCR*, here R_w)		$R_w = \omega_p L$: $f_p = \dfrac{R_w}{2\pi L}$	
	datasheet typical	measured µH	datasheet, typical	measured mΩ	Typical Hz	calculated Hz
L_1	10 µH		21.8 mΩ		347	
L_2	33 µH		61.9 mΩ		299	
L_1+L_2	43 µH		83.7 mΩ		310	
A→B	43 µH					

Listing 3.2.1: *Matlab* computation of frequencies f_{xL} where $R_w = \omega_x L$

```
% Computing the poles of inductors and series resistors
L_datasheet(1)  = 10e-6;  Rw_datasheet(1) = 21.8e-3;
L_datasheet(2)  = 33e-6;  Rw_datasheet(2) = 61.9e-3;
L_datasheet(3)  = L_datasheet(1)  + L_datasheet(2);
Rw_datasheet(3) = Rw_datasheet(1) + Rw_datasheet(2);

L_measured(1) = 10.6e-6;   Rw_measured(1) = 27.45e-3;
L_measured(2) = 32.98e-6;  Rw_measured(2) = 67.0e-3;
L_measured(3) = 42.98e-6;  Rw_measured(3) = 84.3e-3;

% Computing the Poles
for i=1:3;
  fxL_datasheet(i) = Rw_datasheet(i) / (2*pi*L_datasheet(i));
  fxL_measured(i)  = Rw_measured(i ) / (2*pi*L_measured(i));
end;
fxL_datasheet, fxL_measured
```

3.2.2 Measuring Inductor L_1+L_2 (nominal 43µH) with *Bode100*

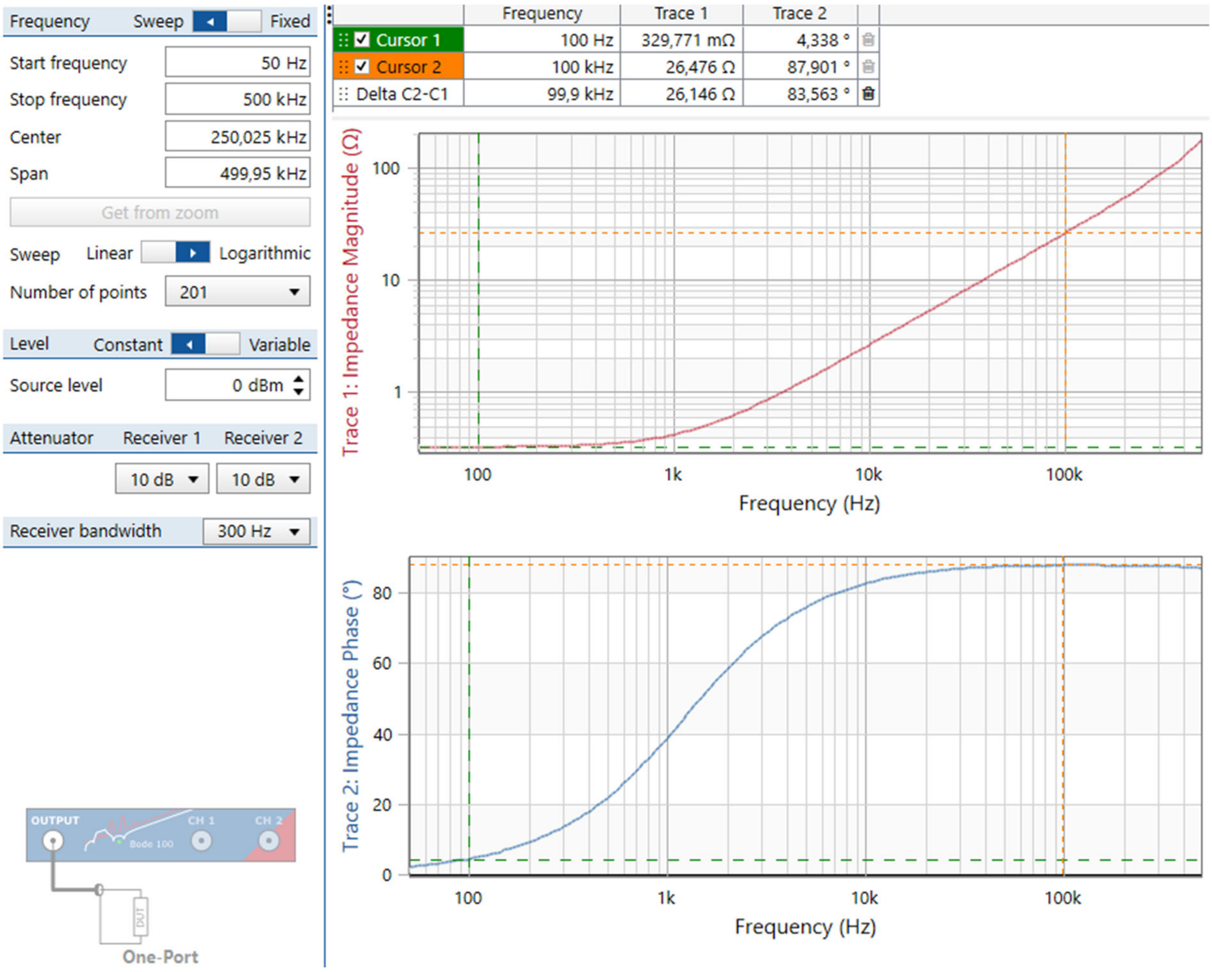


Fig. 3.2.2: *Bode100 One-Port Impedance* measurement of both inductors: (10+33) µH

Summarizing measured results

DCR: at f = 100 Hz: $R_{AB} = R_{meas} - R_{cable} =$

. . . .

L: at f = 100 KHz: $X_L = j\omega L \rightarrow L = \frac{|X_L|}{2\pi f} =$

. . . .

Zero: Phase rises by 45° and R_w begins to play a significant role, for at ca.

. . . .

3.2.3 Measure 680µF-Capacitor and 43µH-Inductor with *Bode100*

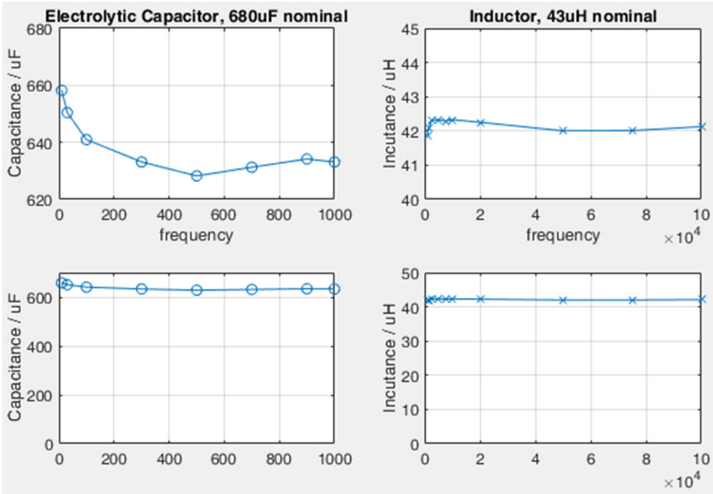


Fig. 3.3: *Bode100 One-Port Impedance* Capacitor and Inductor measured with *Bode100 One-Port Impedance* measurement and computed with *Matlab* code in Listing 3.3.
+ Upper left: $C_{680\mu F}$ zoomed,
+ Lower left: $C_{680\mu F}$ full scale,
+ Upper right: L_{43uH} zoomed,
+ Lower right: L_{43uH} full scale,

- In the Matlab listing below, replace values of Z_{C_abs} with measured impedance of Fig. 3.1.2 in the frequencies given above as vector f_C.
- In the Matlab listing below, replace values of Z_{L_abs} with measured impedance of Fig. 3.2.2 in the frequencies given above as vector f_L. Measure wire resistor R_w at f=100Hz.
- Run the code with *Matlab* to get Fig. 3.3 for your board.

Listing 3.3: *Matlab* code generating Fig. 3.3

```
% Frequency domain characterization of 680uF Capacitor and 43uH-Inductor
clear all; % clear workspace
%
% compute 680uF-capacitor  als function of frequency
RC680uF = 0.198; % seriel resistor
fC      = [10     30     100    300    500    700    900    1000];
ZC_abs = [24.179 8.159 2.491 0.861 0.544 0.411 0.342 0.320];
XC_abs = sqrt(ZC_abs.^2 - RC680uF^2);
C680uF =1./(2*pi*fC.*XC_abs)
subplot(221); plot(fC,C680uF*1e6,'o-'); grid on;
title('Electrolytic Capacitor, 680uF nominal');
xlabel('frequency'); ylabel('Capacitance / uF'); ylim([620 680]);
subplot(223); plot(fC,C680uF*1e6,'o-'); grid on; ylim([0 700]);
ylabel('Capacitance / uF');
%
% compute 43uH-inductor als function of frequency
Rw = 0.330; % wire resistor measured at 100Hz
fL      = [1     1.5     2.5     5     7.5   10    20    50    75    100 ]*1e3
ZL_abs = [0.422 0.516  0.742  1.37 2.02 2.68 5.32 13.2 19.8 26.47];
XL_abs = sqrt(ZL_abs.^2 - Rw^2)
L43uH = XL_abs./(2*pi*fL);
subplot(222);
plot(fL,L43uH*1e6,'x-'); % plot over linear abscissa
%semilogx(find,L_43uH,'x-'); % plot over logarithmic abscissa
title('Inductor, 43uH nominal'); grid on;
xlabel('frequency'); ylabel('Incutance / uH'); ylim([40 45]);
subplot(224); plot(fL,L43uH*1e6,'x-'); grid on; ylim([0 50]);
ylabel('Incutance / uH')
%
% compute oscillation frequency in C, L measured at 1KHz
f0_1KHz = 1/(2*pi*sqrt(C680uF(end)*L43uH(1)))
```

Keep in mind:
- Inductors degrade with current magnitude
- Electrolytic capacitors degrade with frequency
- Ceramic capacitors degrade with DC bias voltage.

3.3 Characterize the *RLC* Series Impedance

Chapter 3.3 delivers an accurate measurement of $f_0 = 1/(2\pi\sqrt{LC})$ and $R_S = R_C+R_D$. Particularly knowing f_0 is helpful for later transfer function calculations and measurements.

Measurement of the small DC resistors in the *RLC* circuit is difficult but important for accurate stability analysis and setting of PID controller parameters. Comparing our 2 measurement methods to get the total series resistor of inductor, capacitor and board wiring, we found:

The next subsections are organized as follows:

1. Subsection 3.3.1 offers the theory for the following 2 subsections.
2. Subsection 3.3.2 measures small values of *Z* with a 2-wire measurement technique that *Omicron* calls "*One-Port Impedance Analysis*", according to Fig. 3.3.1(a): The voltmeter measures also the measurement-cable resistors R_{mc1} and R_{mc2} with high current load.
3. Subsection 3.3.3 measures *Z* with a 4-wire measurement technique that *Omicron* calls "*Shunt-Thru Impedance Analysis*", according to Fig. 3.3.1(b): The voltmeter measures *Z* more precisely, as the 2 additional wires R_{mc3} and R_{mc4} carry very low current.
4. Subsection 3.3.4 compares the measurement results of the previous 2 subsections.

3.3.1 Theory: Computing of $R_S = R_C+R_D$, and $f_0 = 1/(2\pi\sqrt{LC})$

With total serial impedance with total serial resistor $R_S = R_C + R_D$ we get

$$Z_{RLC}(s) = R_S + sL + \frac{1}{sC} = R_S + \frac{1+s^2LC}{sC}$$

and with $s = j\omega$

$$Z_{RLC}(\omega) = R_S - j\frac{1-\omega^2LC}{\omega C}.$$

Consequently, both $R_S = R_C + R_D$ and $f_0 = \omega_0 / 2\pi = 1/(2\pi\sqrt{LC})$ can be taken from the minimum of the shown in Fig. 3.3.2, taken with *Bode100 One-Port Impedance* measurement.

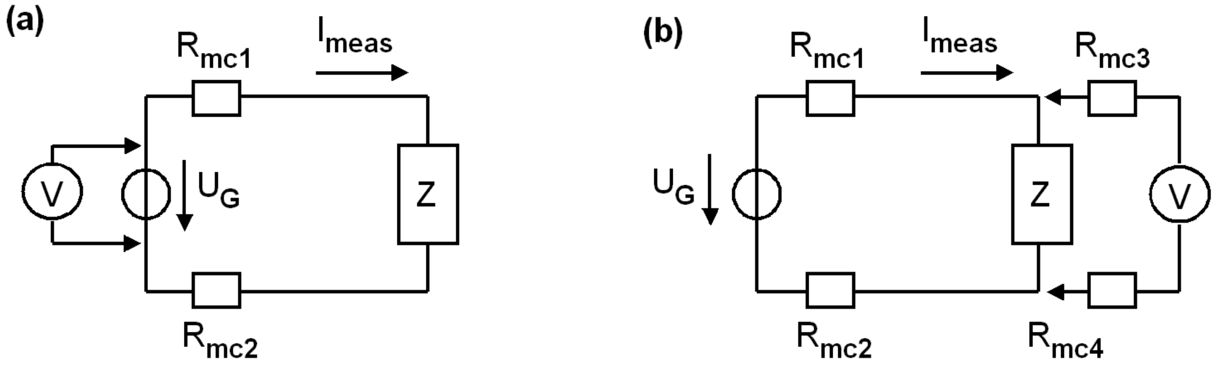


Fig. 3.3.1 (a): 2-wire (*Bode100*: "*One-Port*") and **(b)** 4-wire ("*Shunt-Thru*") measurement

3.3.2 RLC Series One-Port Impedance Analysis

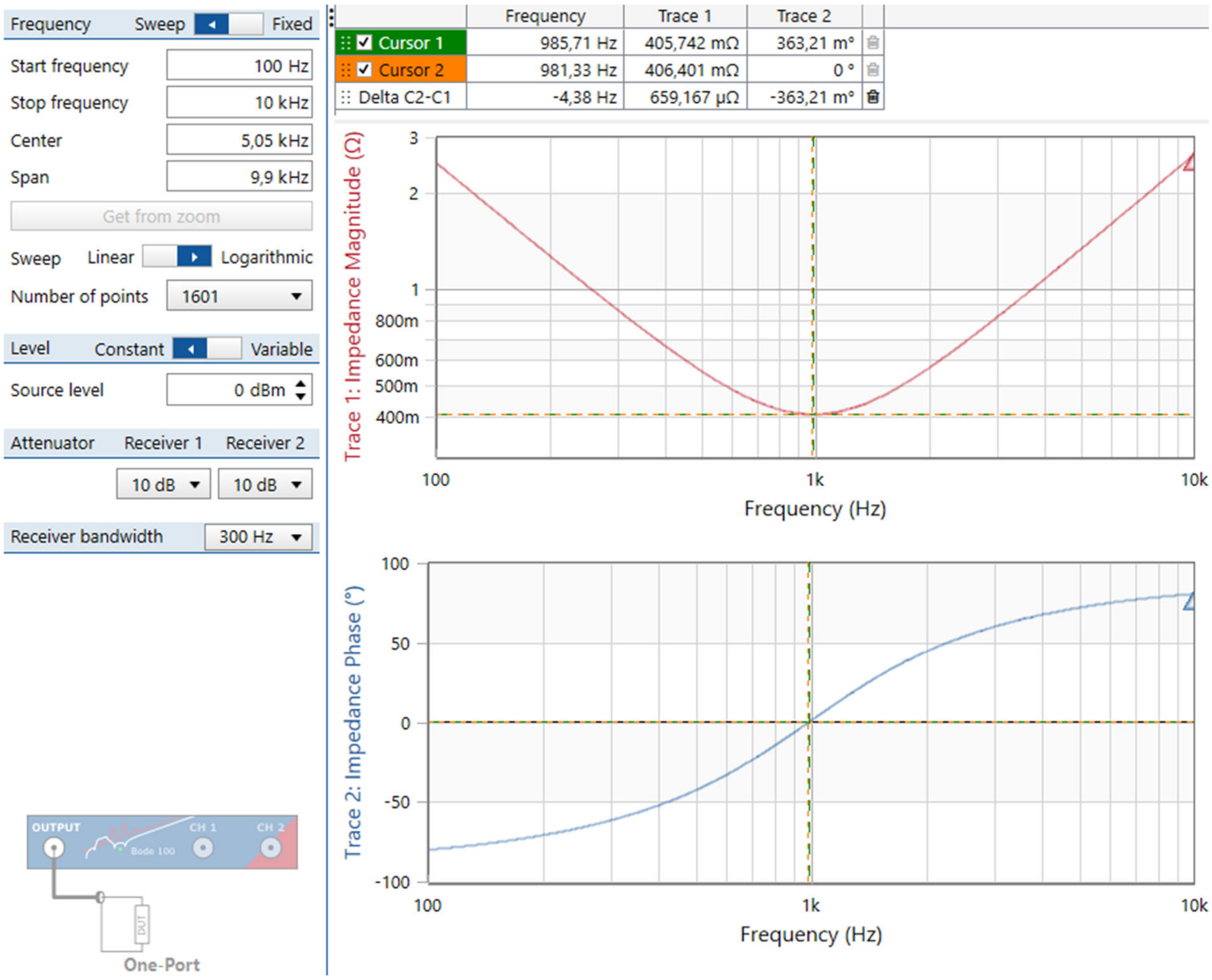


Fig. 3.3.2(a): *Bode100 One-Port Impedance* measurement: point *A* in Fig. 3.0 versus ground.

DCDCbuck board: no jumpers to coils: L=43µH nominal, set jumper for C=680µF nominal. Connect a BNC cable from *Bode100 OUTPUT* to an isolated *DCDCbuck* board's point *A* according to Fig. 3.0 and ground, as sketched in the lower left corner of Fig. 3.2.2(a).

Start *Bode Analyzer Suite* → *Impedance Analysis* → *One-Port / Start Measurement* → frequency range 100Hz – 10KHz and default settings otherwise. Click *Continuous* or *Single*  button to get a measurement. Select *View* → *Auto axis placement* → *One axis per chart*.

Optimize Magnitude diagram:

- Click into *Impedance Magnitude* diagram with right mouse button → *Optimize*.
- *Magnitude* diagram, right mouse button → *Cursor 1* → *Find* → *Minimum (Trace 1)*.

Optimize Phase diagram:

- Click into the *Impedance Phase* diagram with right mouse button → *Optimize*.
- *Phase* diagram, right mouse button → *Cursor 2* → *Find* → *Zero (Trace 2)*.

According to theory, both cursor 1 and 2 should be at the same frequency now. Normally this is not the case. Repeat the measurement detailed above with 1601 points, create your own Fig. 3.3.2(a) with your *DCDCbuck* board and copy it into your documentation.

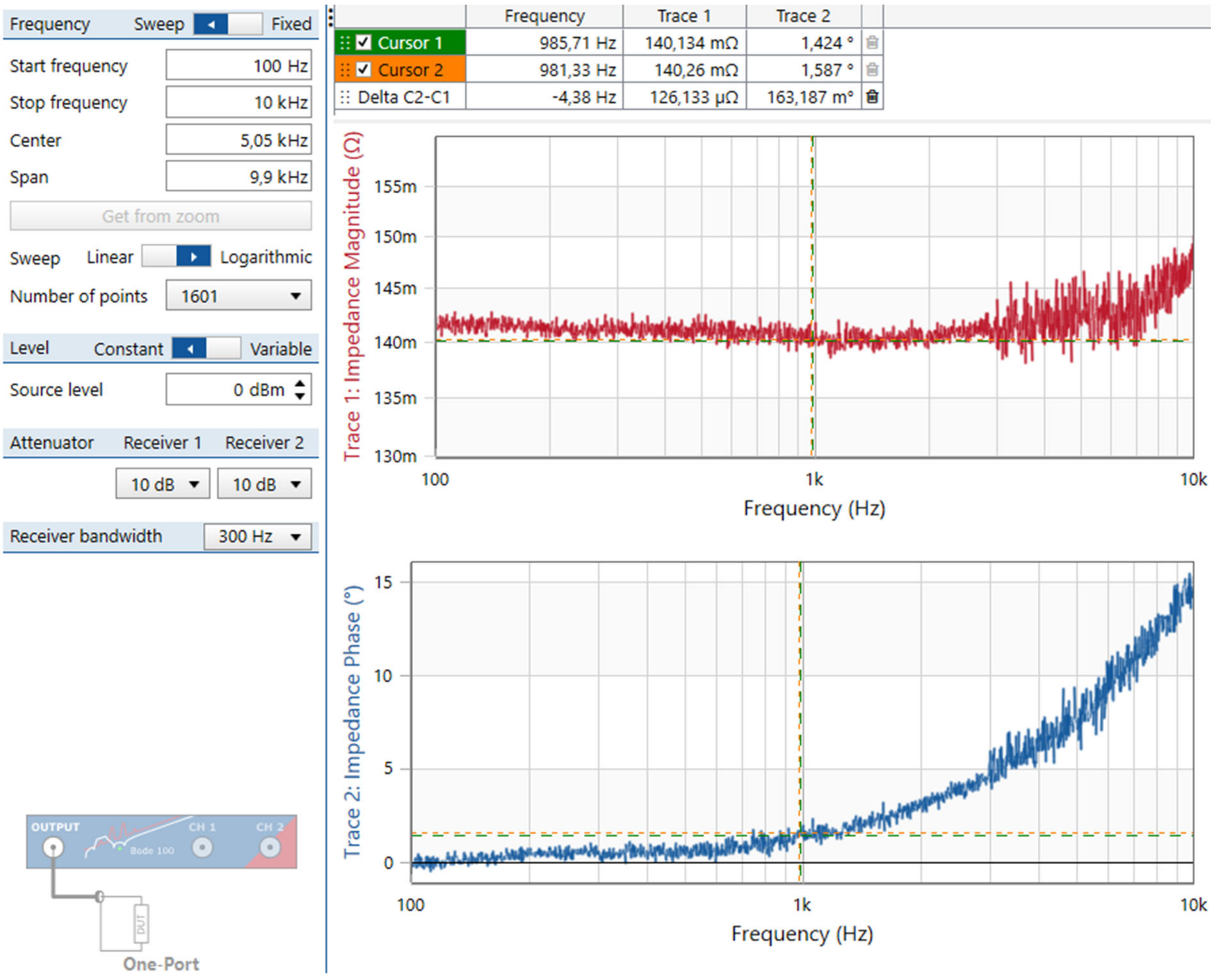


Fig. 3.3.2(b): *One-Port Impedance Measurement* with *Bode100* of a 125cm *BNC-to-pin* cable.

The measurement shown in Fig. 3.3.2(a) includes the cable resistors. <u>To find out the cable impedance</u>, connect both ends of your measurement cable to ground and repeat the measurement of Fig. 3.3.2(a).

Under the cursors that have been set in the measurement above we now find
(i) the cable's resistor part and
(ii) the phase characteristics of the cable, that explains the cursor 2 at phase 0 in Fig. 3.3.2(a) is a little bit left from cursor 1 at impedance magnitude minimum.

Close *Bode Analyzer Suite*, start it again → *Impedance Analysis* → *One-Port*. What is the recommended impedance measurement range? Is it ok for our measurements above?

. . . .

. . . .

Summarize values for board

. . . .

Taken from the minimum of Fig. 3.3.2(a)

f_0 =

. . . .

Taken from the minimum of Fig. 3.3.2(a)

$R_S + R_{cable}$ =

. . . .

Taken from the minimum of Fig. 3.3.2(b)

R_{cable} =

. . . .

$R_S = (R_S + R_{cable}) - R_{cable}$ =

. . . .

3.3.3 RLC Series Shunt-Thru Impedance Analysis

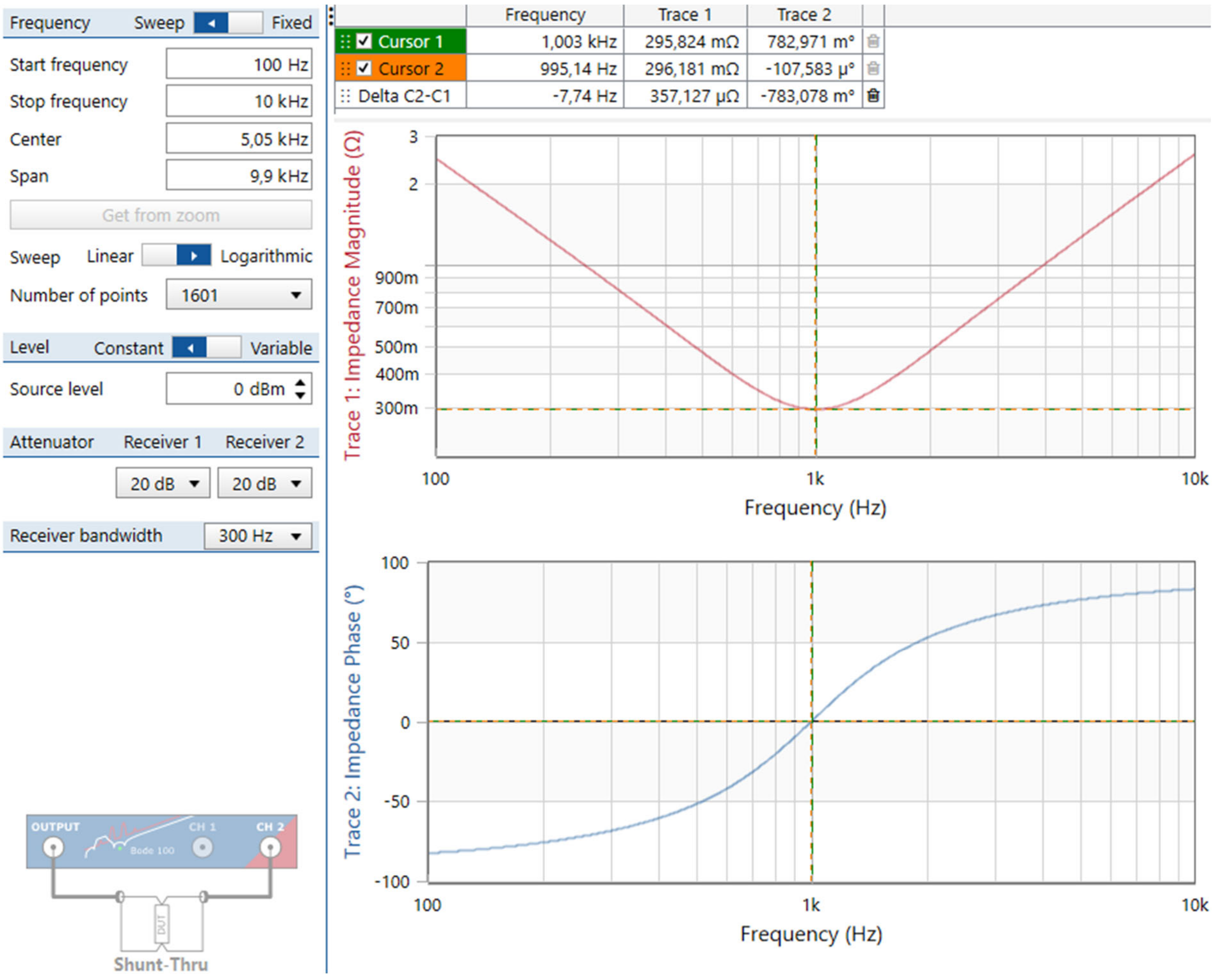


Fig. 3.3.3(a): *Bode100 Shunt-Thru* impedance measurement: point *A* in Fig. 3.0 versus ground.

One-Port Impedance measurement made above is inaccurate from 2 reasons: (i) We measure the cable resistors, and (ii) we are out of the valid (accurate) range of the *Bode100*. For this case, it has the so –called shunt-thru measurement option. Let's try it in this subsection!

Close *Bode Analyzer Suite*, start it again → *Impedance Analysis* → *Shunt Thru*. What is the recommended impedance measurement range? Is it ok for out measurements above?

. . . .

Look at the shunt-thru measurement setup. We now have the problem, that we need to pins at any side of the device under test (DUT). Two ground pins are no problem, but where do we find the 2nd pin on the DCDCbuck board connecting to point *A* in Fig. 3.0? To figure it out open the *DCDCbuck* Rev.5 board schematic and layout with *Eagle* tool, activate *View* → *Show* in the schematics editor and click on the wire connecting the coils at point *A* in Fig. 3.0. Where is the 2nd pin connecting the coils at this point *A*?

. . . .

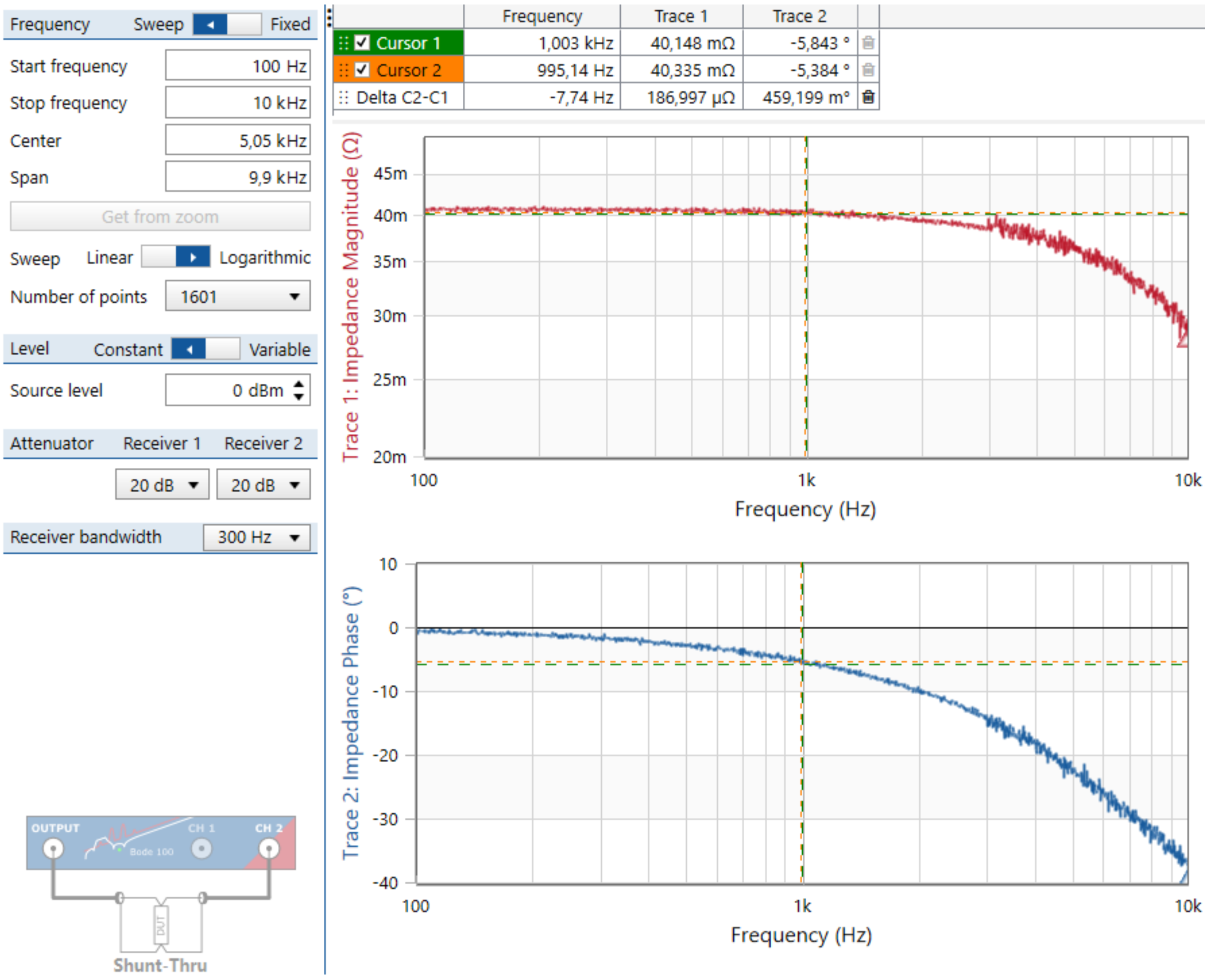


Fig. 3.3.3(b): *Bode100 Shunt-Thru* impedance measurement of cables only

Measure cables only by plugging them all close together on a ground connector.

Impedance at minimum in Fig. 3.3.3(a): R_{tot} = ... at f_0 = ...

Cable characteristics at f_0 in Fig. 3.3.3(b): R_{cable} = ... , Phase = ...

Total series resistor $R_S = R_C + R_D = R_{tot} - R_{cable}$ = ...

3.3.4 Summary of *RLC* Series Measurement in this Subsection 3.3:

Measurement of the small DC resistors in the RLC circuit is difficult but important for accurate stability analysis and setting of PID controller parameters. Comparing our 2 measurement methods to ret the total series resistor of inductor, capacitor and board wiring, we found:

In chapter 3.3.2 with *Bode100's Series One-Port Impedance* Analysis we got:

total series resistor is $R_S = R_C + R_D =$ . . . . at resonant frequency $f_0 =$ . . . .

In chapter 3.3.3 with *Bode100's Shunt-Thru Impedance* Analysis,

total series resistor is $R_S = R_C + R_D =$ . . . . at resonant frequency $f_0 =$ . . . .

3.4 RLC-Lowpass Transfer Function (*PTF*)

In this subsection we shall investigate the resonant behavior of the RLC lowpass. Doing so, we shall understand the impact of the small DC resistors measured in subsection 3.3.

3.4.1 Measurement Using *Bode100 Transmission* mode

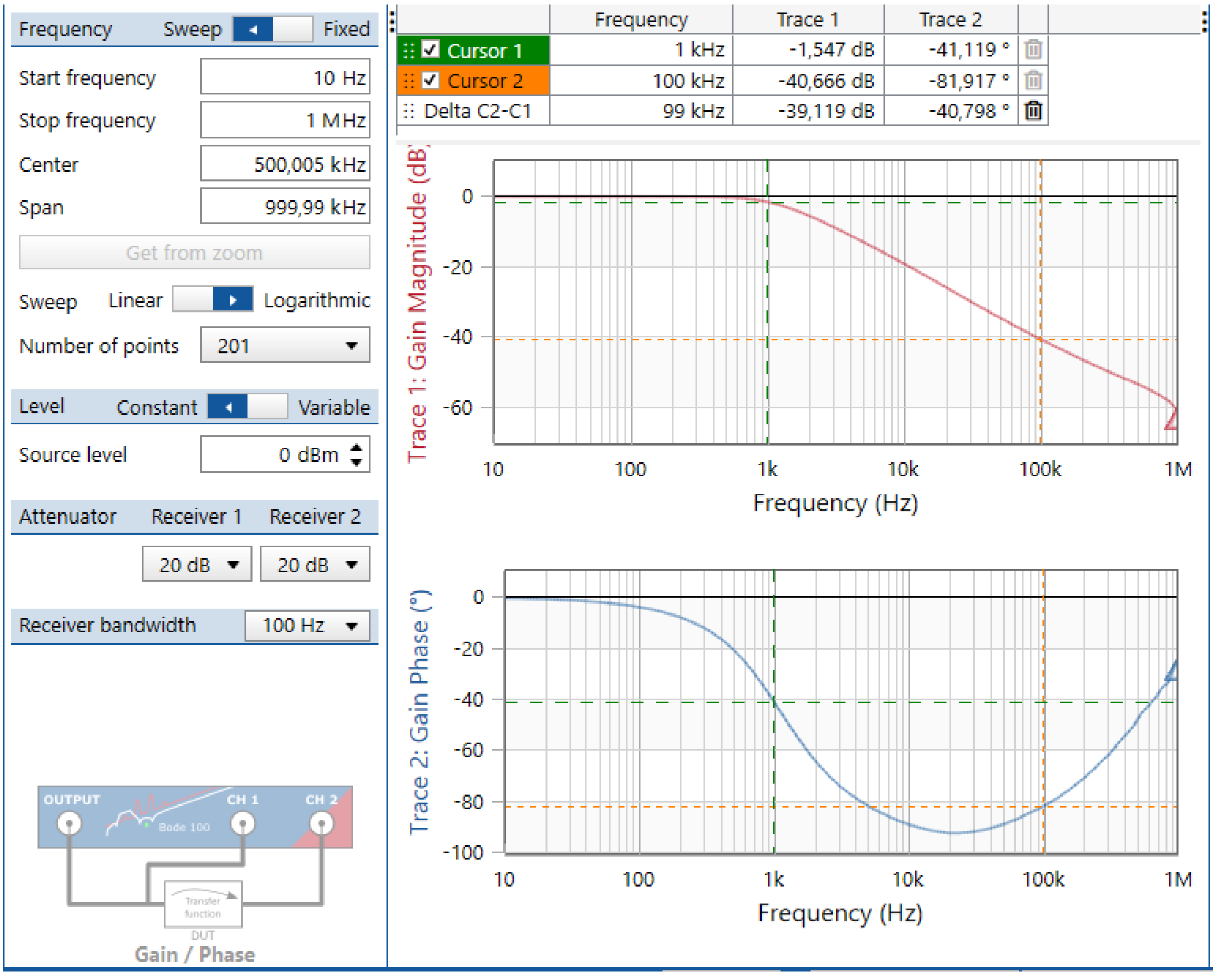


Fig. 3.4.1: Process Transfer Function (*PTF*) of the *RLC* lowpass measurement with *Bode100* as *Gain/Phase* measurement. The cursor is at f_0 measured with impedance analysis.

Fig 3.4.1 shows a measurement performed with *Bode100* of the *RLC* lowpass from point *A* to point *B* in Fig. 3.0, with *DCDCbuck* board (Rev.5) being disconnected from any other device.

- Cursor 1 is at the position measured as f_0 in the impedance analysis above.
- Cursor 2 is near a zero at $f_n \approx 4$ KHz in the transfer function caused by R_C. That zero compensates for one of the double-poles (at 1KHz) for $f > f_n$. Consequently, attenuation for f >>10 KHz is 1st order only.

This lowpass transfer function corresponds to box *Process* in Fig. 1.1.

To do:
Measure your own version of Fig. 3.4 for your individual *DCDCbuck* board.
Save your *Bode100* measurement file as *OL1_DCDCbuckRev10_RLC.bode3*.

3.4.2 Computing DC Resistor R_D

(a) System setup

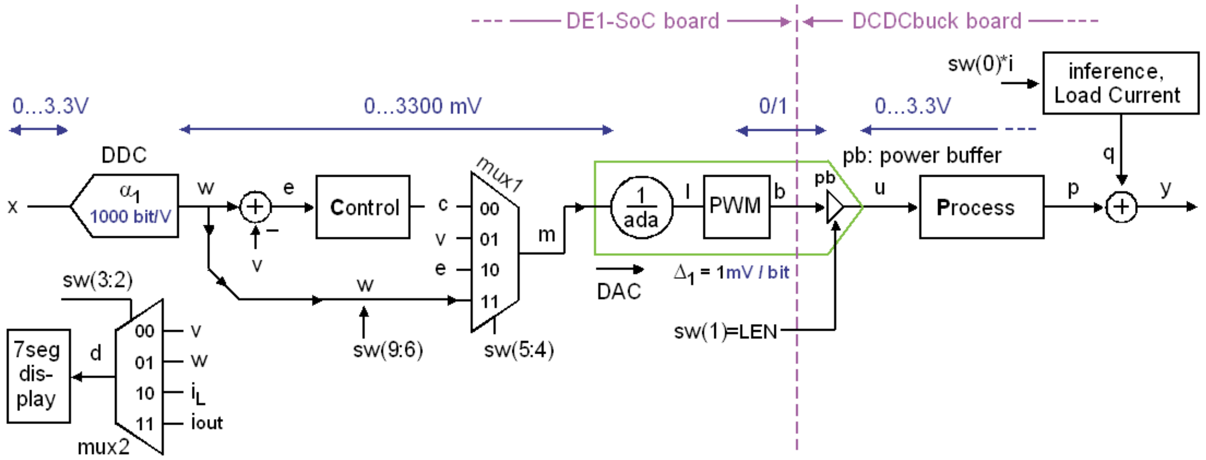
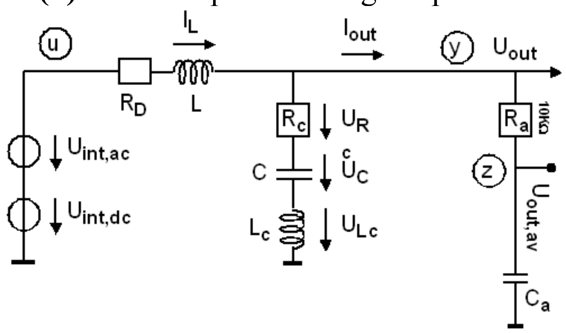


Fig. 3.4.2:

(a) System setup

(b) Assuming the main *RLC* lowpass to be driven by an inner DC source $U_{int.dc}$ in series with an AC source $U_{int.ac}$. Output ripple voltage is removed on the average output voltage $U_{out,av}$ by low-pass filtering.

(b) *RLC* low-pass forming the process



According to Fig. 3.4.2 we model the PWM driver as DC source $U_{int.dc}$ plus AC source $U_{int.ac}$. The effect of the AC source is largely eliminated by the *RLC* low-pass filter, so that we can measure $U_{int.dc}$ as average output voltage at zero load current. After switching on the load current I_{out}, the average output voltage $U_{out.av}$ decreases by $R_D{\cdot}I_{out}$.

Set *sw* = "0000 11 00 10" to get *w*=1250mV, fixed pulse-width and synchronous operation.

Measure at sw(0)='0' : **Uint,dc = Uout,av,OFF = ______ mV, Iout,OFF = ______ mA,**

Measure sw(0)='1' : **Uout,av,ON = ________ mV, Iout,ON = ______ mA,**

Compute RD(w=1250mV) = $\dfrac{U_{int,DC} - U_{out,av}}{I_{out,ON} - I_{out,OFF}} =$ ______________________________ **Ω.**

Hint: R_D should be in the range of 140…160 mΩ.

3.4.3 Calculation of Characteristic Data Using Matlab

Listing 3.4.3 computes some key parameters such as poles (index p) and zeros (index n) for the transfer function *PTF(s)*=$U_{out}(s)/U_{in}(s)$ and inference (quarrel) transfer function *QTF(s)*=$U_{out}(s)/I_{out}(s)$. Run the file with Matlab, adopt key input data (L, C, …) to your board.

Listing 3.4.3: *Matlab* code generating Fig. 3.4

```
% Computation of characteristic data of an RLC lowpass
%  A: Input, B: outout
%  A -> B: inductor L serial with RD=Rw+Rb, Rw: wire, Rb: board
%  B -> gnd: capacitor C with seriel resistor RC
clear all;  % clear workspace
%
pi2 = 2*pi;
Rb=0; % other board impedances from point A to point B
L   = 43e-6; Rw=83.7e-3; % Inductor
RD  = Rb + Rw; % DCR: total DC resistor from A -> B
C   = 640e-6; RC=0.06;   % capacitor
%
ap0=1; ap1=RC*C; ap2=0;
bp0=1; bp1=(RC+RD)*C; bp2=L*C;
%
% Computing PTF=Uout/Uin: Process transfer function
w02 = 1/(L*C);          % squared w0
w0 = sqrt(w02);         % undamped oscillation frequency
f0 = w0/pi2;
Da = (RC+RD)/(2*L);     % absolute damping term
D  = Da/w0;             % damping term relative to w0
spn1 = -1/(RC*C);       % PTF, zero 1 in rad/sec
spn2 = -inf;            % PTF, zero 2 in rad/sec
fpn1 = abs(spn1)/pi2;   % PTF, zero 1 in Hz
fpn2 = abs(spn2)/pi2;   % PTF, zero 2 in Hz
if Da^2 > w02;
  spp1 = -Da+sqrt(Da^2-w02);  % PTF, non oscillating pole 1
  spp2 = -Da-sqrt(Da^2-w02);  % PTF, non oscillating pole 2
else
  spp1 = -Da+j*sqrt(w02-Da^2); % PTF, oscillating pole 1 in rad/sec
  spp2 = -Da-j*sqrt(w02-Da^2); % PTF, oscillating pole 2 in rad/sec
end;
spp1_abs = abs(spp1); spp1_ang=angle(spp1); spp1_deg=spp1_ang*180/pi;
spp2_abs = abs(spp2); spp2_ang=angle(spp2); spp2_deg=spp2_ang*180/pi;
fpp1 = spp1_abs/pi2; % PTF, pole 1 in Hz
fpp2 = spp2_abs/pi2; % PTF, pole 2 in Hz
%
% Computing QTF=Uout/Iout: inference (Quarrel) transfer function
aq0=-RD; aq1=-(RC*RD*C+L); aq2=-RC*L*C;
bq0=bp0; bq1=bp1;          bq2=bp2;
sqn1 = -aq1/(2*aq2) - sqrt((aq1/(2*aq2))^2-aq0/aq2); % zero 1, rad/sec
sqn2 = -aq1/(2*aq2) + sqrt((aq1/(2*aq2))^2-aq0/aq2); % zero 2, rad/sec
sqp1 = spp1; % poles are the same as for PTF
sqp2 = spp2; % poles are the same as for PTF
% translation from rad/sec -> Hz
fqn1 = abs(sqn1)/pi2;   % QTF, zero 1 in Hz
fqn2 = abs(sqn2)/pi2;   % QTF, zero 2 in Hz
fqp1 = fpp1;            % QTF, pole 1 in Hz
fqp2 = fpp2;            % QTF, pole 2 in Hz
%
% plot Bode diagram, if DSP toolbox is available
dsp_toolbox_available = 0; % set this to 1 if dsp toolbox avaialble
if dsp_toolbox_available == 1;
  TFP = tf([ap2,ap1,ap0],[bp2,bp1,bp0]);
  opt=bodeoptions; opt.FreqUnits='Hz'; opt.grid='on';
  bodeplot(TFP,opt);
end;
```

3.5 DC Output Resistor of Complete PWM-DAC

Goal of this subsection: Measure the DC output impedance of the complete PWM-DAC consisting of digital pulse-width modulator, power FETs and RLC-lowpass as demodulator.

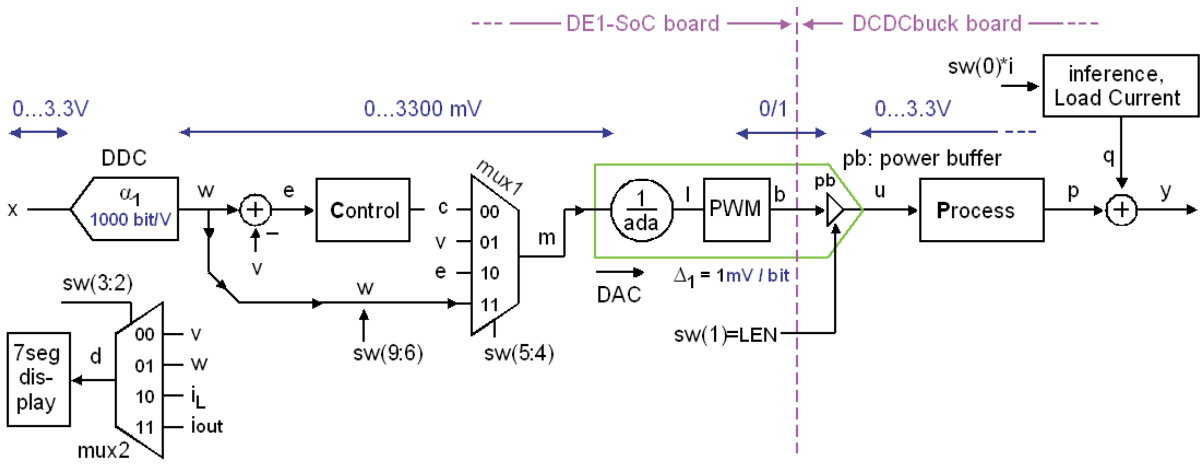


Fig. 4.2.1: The DC/DC buck converter setup for the measurements of this chapter.

What makes PWM DACs energy efficient?

The modulator's power stage is efficient, because its switches are either ON of OFF. The loss heating the switches is $P_V = U_S \cdot I_S$ with U_S being voltage across and I_S current through the switch. U_S or I_S are tiny in *ON* and *OFF* state, respectively. The averaging demodulator following the modulator is ideally an *LC* lowpass, whereas both inductor *L* and capacitor C are lossless in the ideal case. Practically, the lowpass has inevitably resistors. On the one hand these resistors lower efficiency, on the other hand they damp oscillations. The oscillating nature of a weakly damped *RLC* lowpass must be compensated for by a control unit.

Explaining the setup

We want to investigate the complete PWM-DAC, which consists of a PWM modulator (realized on the FPGA) as factor 1/*ada* and modulation logic ("PWM"). On the *DCDCbuck* board the PWM modulator is completed by a power buffer (*pb*) with input signal "*sw(1) = LSE = LEN*". The PWM demodulator is the *RLC* lowpass labeled "*Process*".

With *w* = 1500, the output pulses of the PWM has a duty cycle of 150/300, i.e. 150 of the *pwm_period* = 330 bits of an output sample are high, while the remaining 180 bits are low. Feeding the PWM power buffer with power gnd/U_{in} = 0/3.3V in Fig. 4.0(d), the average output of the PWM-DAC is ideally 1.5V. This is the voltage that we expect to measure at the output of the averaging lowpass.

Set the following 3 jumpers:

- Set jumper on DCDCbuck board to 3.3V supply achieving the same pulse height.
- A further jumper connects the 680µF capacitor to the output the board.
- Set jumper JP_ASYNC to enable the *Schottky* diode.
- Remove jumper *JP_LOAD* as we will load the circuit externally.

Set switches

For starting set sw(9:0)="0110 **11** 10 1 0" ,
— index: 9876 **54** 32 1 0

sw(0)='0': no load current (We will use external current loads)
sw(1)='1': synchronous, '0': asynchronous operation
sw(2)='0': (display modes that we do not need here)
sw (3)='0': if you want to see wanted output *w* on the 7-segment display in mV or
= '1': if you want to see measured output *v* on the 7-segment display in mV.
***sw*(5:4)="11"** during this measurement. This feeds *wanted* output (*w* in Fig. 4.1) directly to the DAC. The division by factor *ada* is required to compensate for differences in ADC and DAC amplifications.
***sw*(9:6)**: set the *wanted* output (*w* in Fig. 4.1) in steps of 250mV.

Comment: sw(1) is the *LEN* = *LSE* (low-side switch enable) signal of *TI's LM27222* [LM27222] chip, causing so-called "synchronous" operation of the DC/DC converter: both power-switches, i.e. pull up and pull down, will operate actively. In the asynchronous mode (*LEN* = '0') the low-side driving switch (S_L) is inactive and its functionality is taken over by *Schottky* diode D_S in Fig. 4.0(d)

Table 4.1: Measuring DC output resistor R_D during *DCDCbuck* board operation

Board #:			**Measurements without feedback: -> sw(5:4)="11"**								
Set:	**Set-**		**Synchronous [sw(1)='1']**						**Asynchronous: sw(1)='0'**		
sw	**point**		U_{out_s0}	U_{out_ss1A}	U_{out_sd1A}	R_{Dss}	R_{Dsd}		U_{out_a0}	U_{out_as1A}	R_{Das}
(9:6)	w/mV		$I_{out} = 0$	$I_{out} = +1A$	$I_{out} = -1A$				$I_{out} = 0$	$I_{out} = +1A$	
			DCDCb.	DCDCboard	DCDCboard	sync	sync		DCDCb.	DCDCboard	async
			unloaded	sources I_{out}	drains I_{out}	src	drain		unloaded	drains I_{out}	src
0000	0										
0001	250										
0010	500										
0011	750										
0100	1000										
0101	1250										
0110	1500										
0111	1750										
1000	2000										
1001	2250										
1010	2500										
1011	2750										
1100	3000										
1101	3250										

Oscilloscope

Trigger PWM pulses on *pin1* of JP1 on *DE1-SOC* board on channel 1 of your oscilloscope.
Observe the DCDCbuck board's output voltage on channel 2 of your oscilloscope.
Both channels should have same scaling and same ground line on the screen.
Use Oscilloscopes *Measure* menu to measure "*DC, N-Cycles*" of CH2.

Unloaded Measurements with *DCDCbuck* board

Set *sw*(1)='1' (=synchronous operation) without load current.
Set switches *sw*(9:6) = "0000" … "1101" corresponding to 0 … 3250 mV. Verify this value with *sw*(3)='0'. Then observe U_{out_s0} of *DCDCbuck* board with *sw*(3)='1'. Note (in table 4.1 or the respective Excel sheet) the measured value taken with a voltmeter (e.g. oscilloscope's DC voltage measurement).

Try the same measurement with asynchronous operation, i.e. *sw*(1)='0'. You will hardly get a meaningful result. You may note them in column U_{out_a0}.

Load Stress Measurements

DC output resistors R_{Dxy} will be measured with

- $x = s$: synchronous operation (*LEN*='1'), $x = a$: asynchronous operation (*LEN*='0')
- y = s: sourcing ($I_{out} > 0A$), y = d: draining: ($I_{out} < 0A$).

Sourcing Load Stress: *DCDCbuck* board sources current: I_{out} = +1A

Set *sw*(1)='1' (=synchronous operation).
Connect a current sink draining I_{out}=1A (if possible), to that *DCDCbuck* board is sourcing 1A.
Set switches *sw*(9:6) = "0000" … "1101" corresponding to 0 … 3250 mV. Verify this value with *sw*(3)='0'. Note the measured output voltages U_{out_ss1A} taken with a voltmeter and compute $R_{Dss} = U_{out\_ss1A}$ / 1A.

Do the same measurement with asynchronous operation, i.e. *sw*(1)='0'. Note the measured output voltages U_{out_as1A} taken with a voltmeter and compute $R_{Das} = U_{out\_as1A}$ / 1A.

Draining Load Stress: *DCDCbuck* board drains current: I_{out} = -1A

Prepare **a current source that never enforces more than 3.5V**! To do so, set 3.5V on an unloaded voltage source, then shorten the output and regulate current to 1A.

Set *LEN* = *sw*(1) = '1' (=synchronous operation only!).
Connect a current source sourcing I_{out}= -1A but, to that *DCDCbuck* board is draining 1A.
Set switches *sw*(9:6) = "0000" … "1101" corresponding to 0 … 3250 mV. Verify this value with *sw*(3)='0'. Note the measured output voltages U_{out_sd1A} taken with a voltmeter and compute $R_{Dsd} = U_{out\_sd1A}$ / 1A.

Do not try the same measurement in asynchronous mode, i.e. *sw*(1)='0'. Forcing current into the output at asynchronous mode will destroy the board, as it cannot drain/sink current in this mode. Remember that the *DCDCbuck* board was already overwhelmed with no output current!

Use Excel to illustrate curves of the different DC output resistors R_{Dxy} of the circuit.

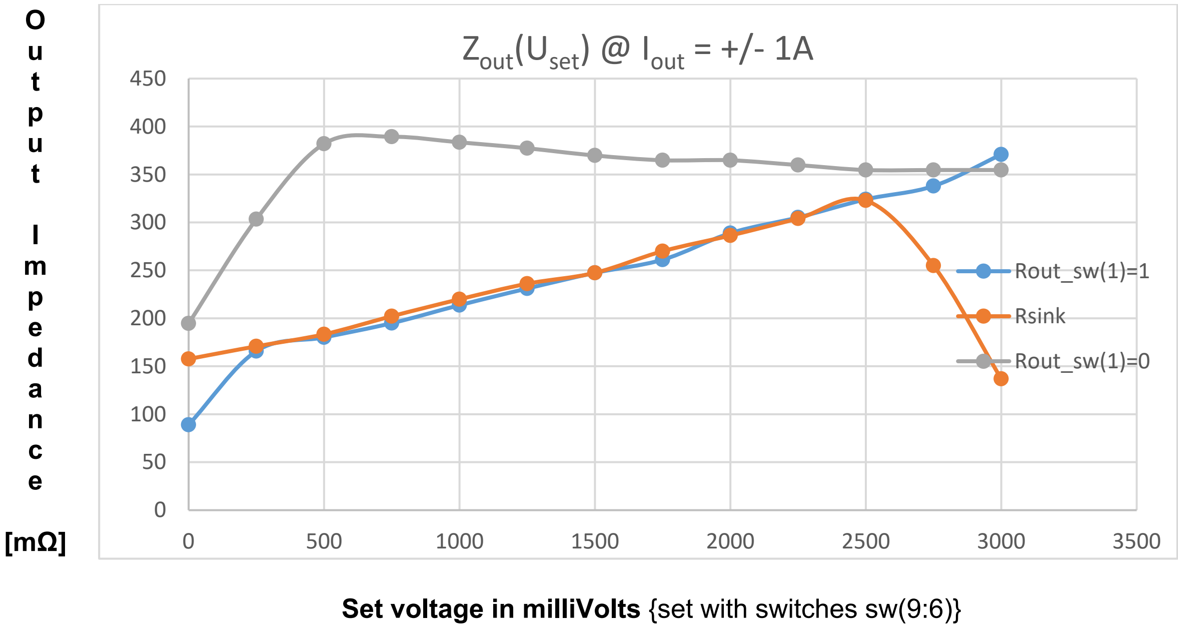


Fig. 4.2.2: DC output impedances measured for a *DCDCbuck* circuit in 3 different modes of operation: blue: synchronous current source, yellow: synchronous current sink/drain, grey: asynchronous current source. Measured was the voltage drop from I_{out}=0 to ±1A.

~~**Interpretation of the measured results:**~~

~~For synchronous operation mode, in the range from w=250…2500 (mV, wanted) for sourcing (R_{Dss}, blue in Fig. 4.2.2) and draining (R_{Dsd}, orange in Fig. 4.2.2) current we get approximately the same DC output resistor, e.g. 250 mΩ at w = 1500 mV.~~

~~Below w=250 the high-side switch becomes more conductive (blue curve down, i.e. R_{Dss} down);~~

~~Above w=2500 the low-side switch becomes more conductive (orange curve down: R_{Dsd} down).~~

~~For asynchronous operation mode the DC/DC converter operates as source current only, as diode D_S in Fig. 4.0(d) cannot conduct current in reverse direction. It is seen that output DC resistor for sourcing currents is higher than for synchronous mode. We assume that this is due to the higher forward resistor of diode D_S compared to open switch (=power-MOSFET) S_L.~~

~~In asynchronous operation the low-level of the PWM signal is V_{pwmL} = –U_{DSF}, with U_{DSF} being the forward bias voltage of diode D_S.~~

~~We now have a figure of the DC/DC buck converters output DC resistor, R_{Dxy}, when the input of the RLC lowpass is fed "embedded" in the system by the PWM power-output buffer (S_H, S_L, D_S). According to Fig. 4.2.2 using gnd/U_{in} = 0/3.3V, I_{out} = ±1A, R_{Dxy} is some~~

- ~~100…325 mΩ for synchronous operation, and~~
- ~~200…400 mΩ for asynchronous operation.~~

~~Is was found in the Master thesis of Thierry Assopguimya by simulation of oscillation behavior [Assopguimya 2020], that R_{Dsy} might be smaller for smaller output currents.~~

4 Conclusions

The passive components of a DC/DC buck converter were characterized with respect to several aspects.

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