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Characterizing Loop Gains of a DC/DC Buck Converter with Digital Voltage-Mode Control

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Practical Training using Board *DCDCbuck_Rev12*

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Abstract. Optimal PID frequency compensation of a digitally controlled DC/DC buck converter.

1 Introduction

1.1 Objectives

Goal of this practical training is to characterize the loop gain and set the digital PID frequency compensation unit of a DC/DC buck converter.

1.2 The *DCDCbuck* Daughter Board Hardware

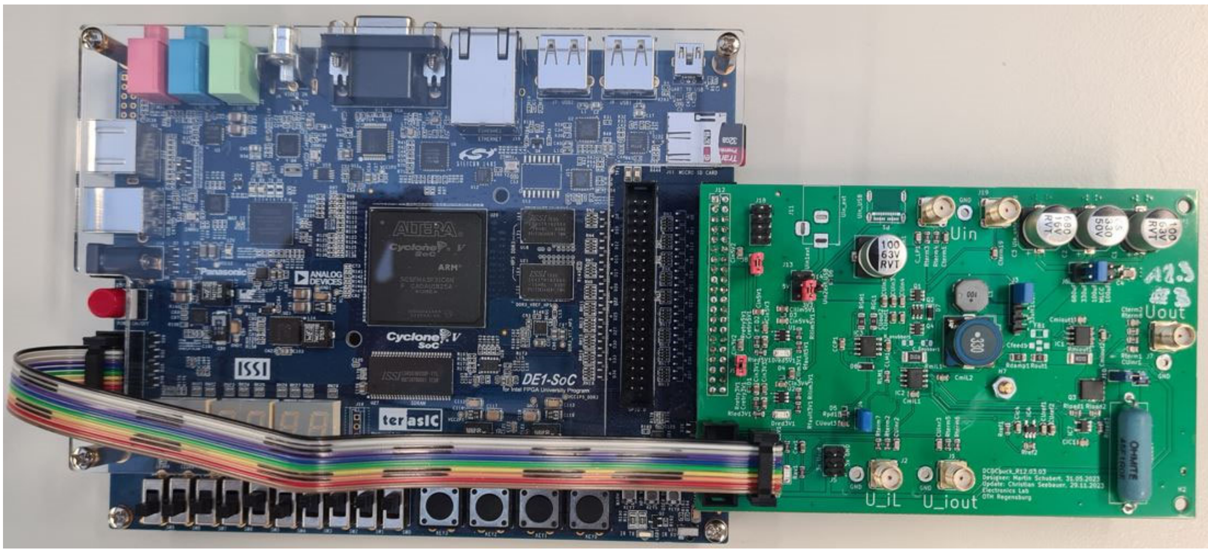


Fig. 1.1: *DE1-SoC* board (left) with plugged-in *DCDCbuck_R12.03* daughter board (right).

Fig. 1.1 shows the *DE1-SoC* board from Terasic [1-8] with *DCDCbuck_Rev10.02.06* daughter board fabricated by Florian Schwankner [10] in the Electronics Laboratory. The ribbon cable connects the input of the *DE1-SoC* on-board's *LTC2308* ADC [15] with output pins of the *DCDCbuck* boar

(a) Board photo, jumpers: red: power, blu: settings, grn: optional

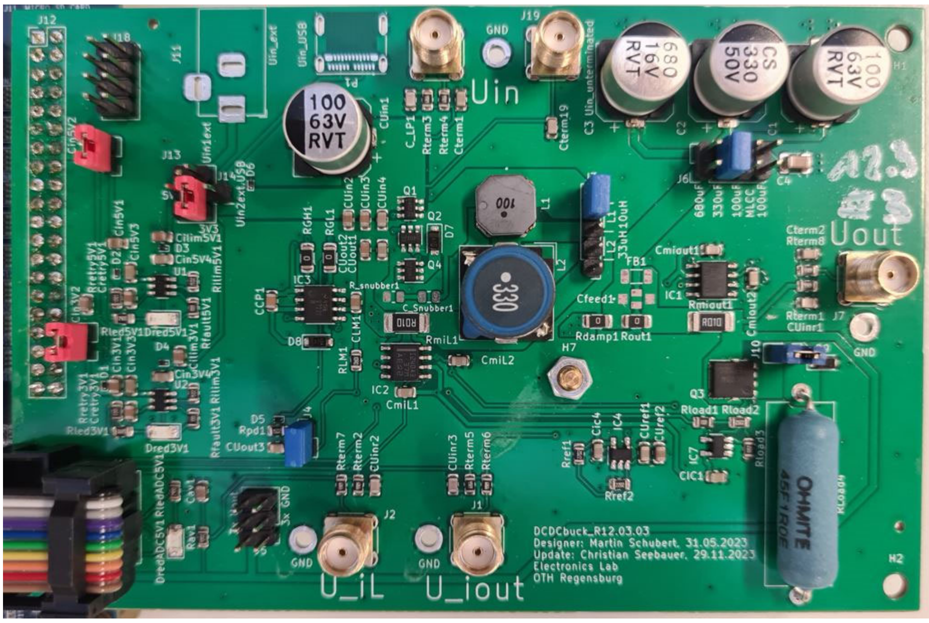


Fig. 1.2: daughter board *DCDCbuck Rev12.03.03*

Bord numbering scheme: *Rxx.yy.zz*, with
xx: Design/Designer, *yy*: No. of fabricated board, *zz*: No. of schematics update of design yy.

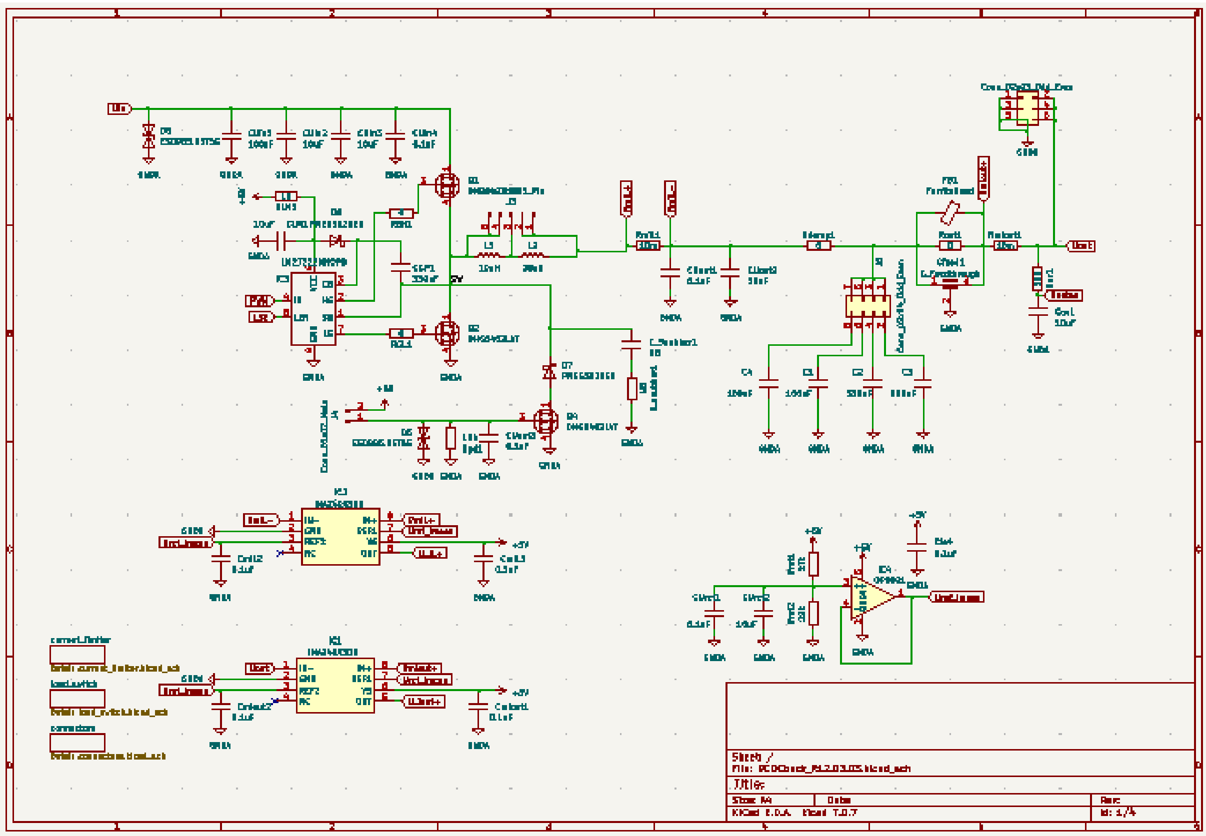
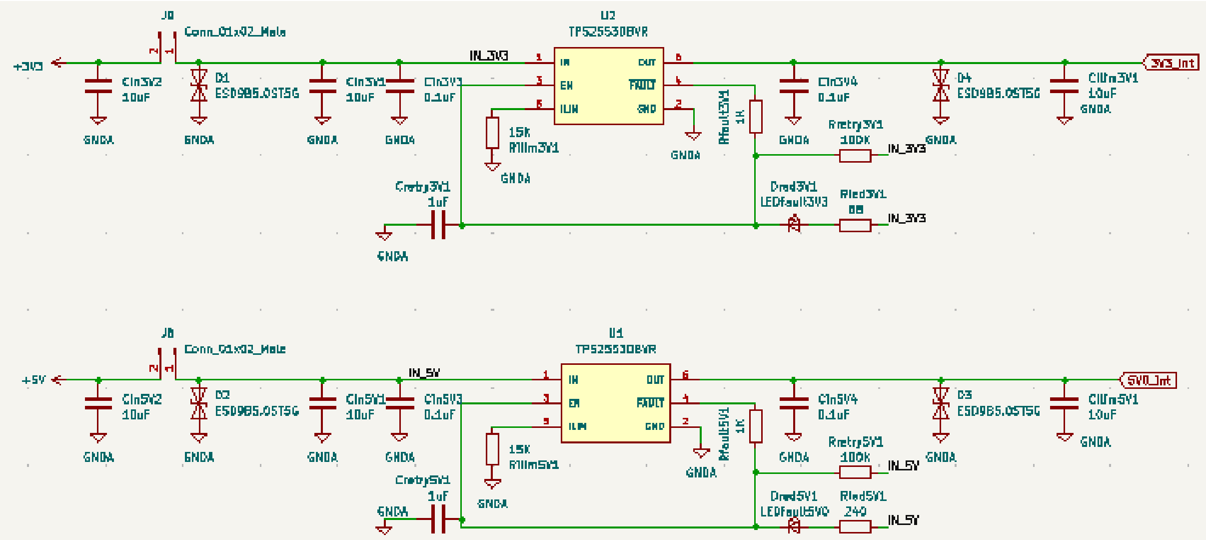
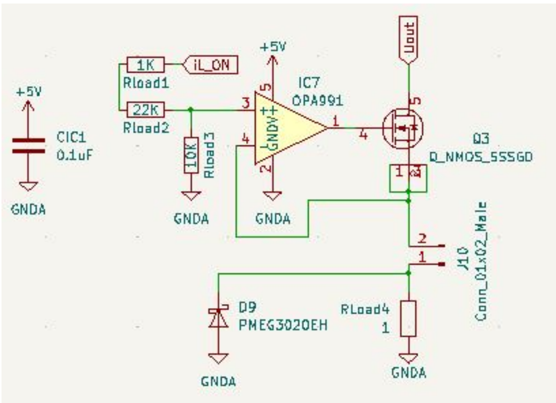


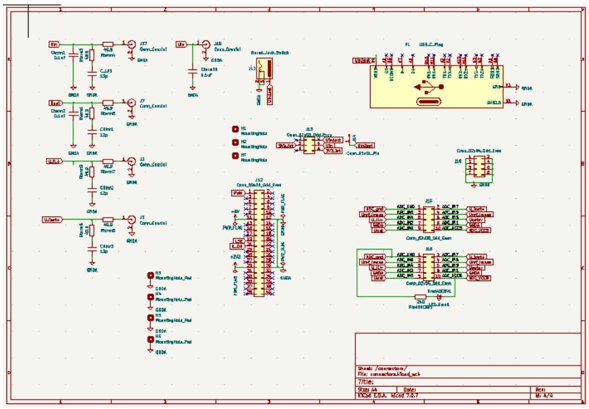
Fig. 1.3(a): *DCDCbuck_R12.03* board top level schematics (in *KiCad* software [19])



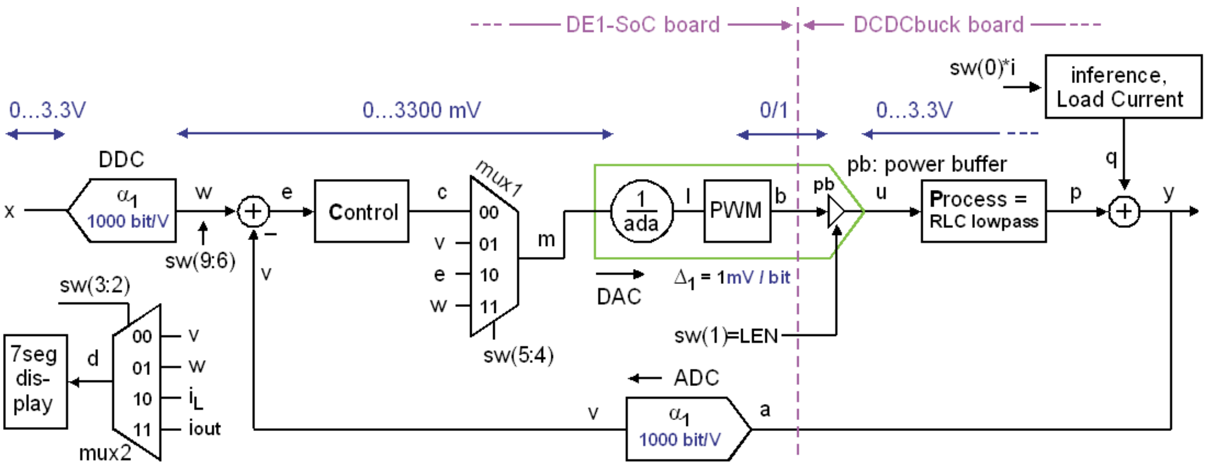
(b): *DCDCbuck_R12.03* board, subcircuit power supplies



(c) Subcircuit 1A Load Current



(d) Subcircuit Connectors



(e) Principal schematics of the DCDCbuck_R12.03 daughter board

Fig. 1.3: *DCDCbuck_R12.03* board, main circuit and subcircuits

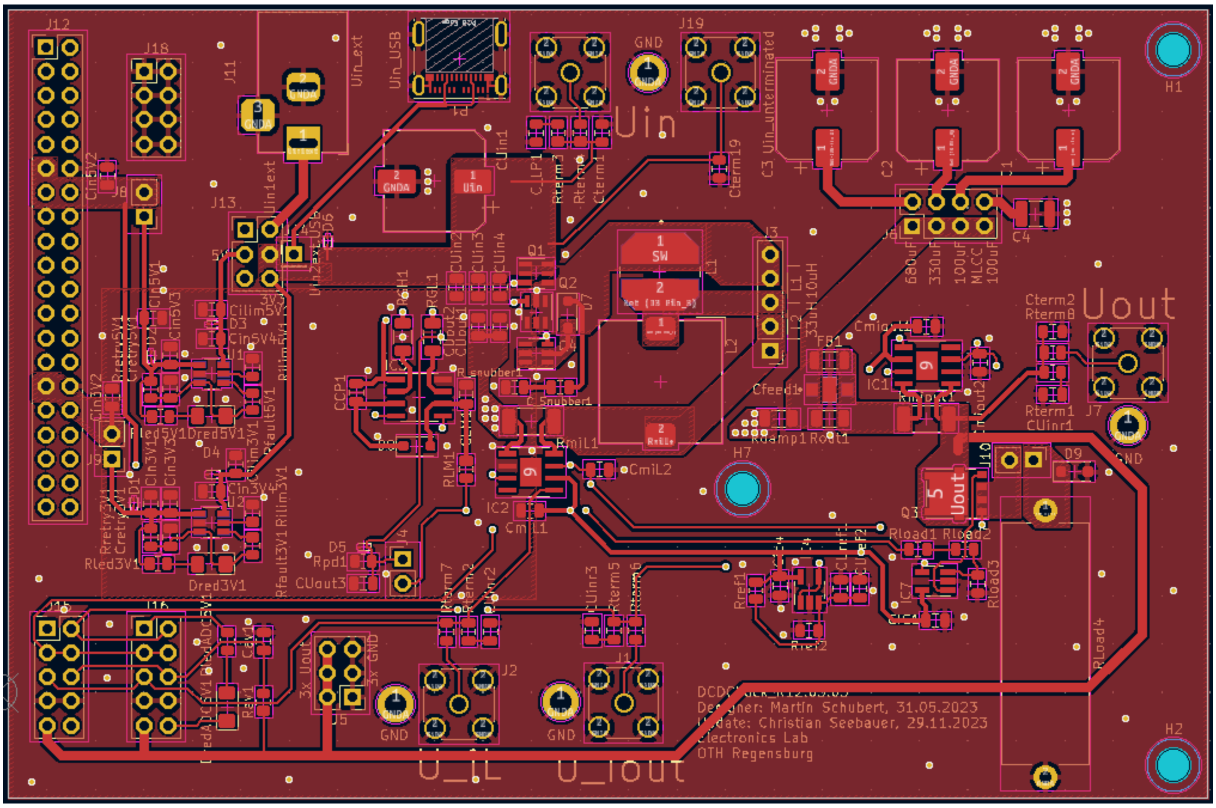


Fig. 1.4(a): *DCDCbuck_R12.03* front-side copper layer (*KiCad* [19])

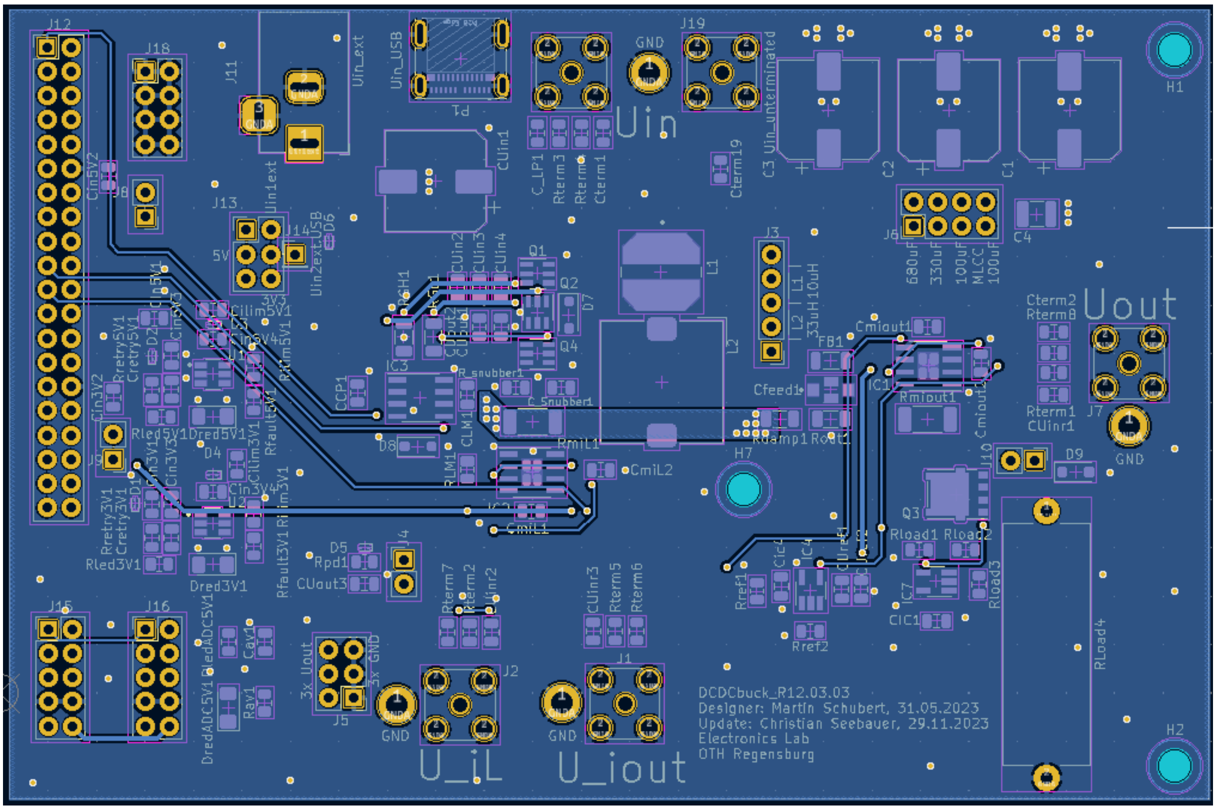


Fig. 1.4(b): *DCDCbuck_R12.03* back-side copper layer (*KiCad* [19])

Fig. 1.4 illustrates the layout (a) and photo (b) of the *DCDCbuck_Rev12.03.03* board. Vias connect different metal layers and may hold pins of plugs.

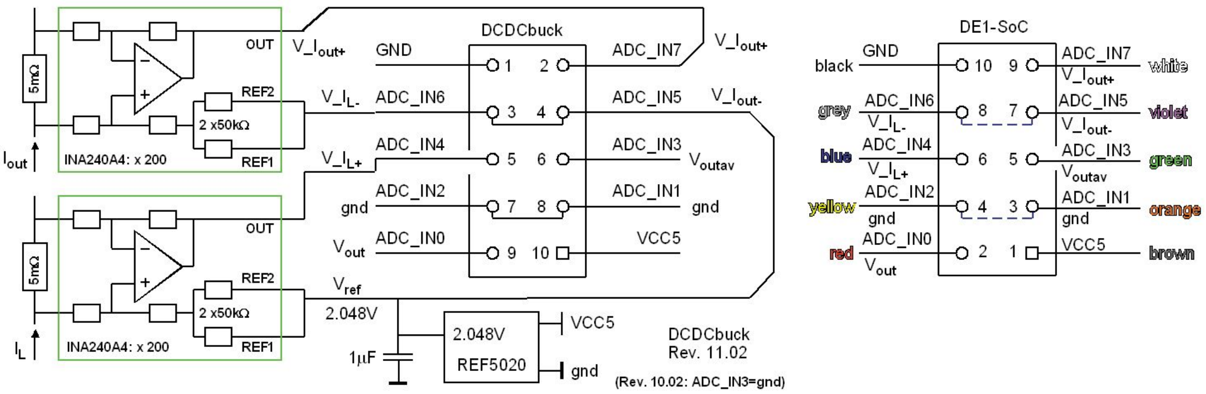


Fig. 1.5: Pin assignment of the 10-pin ADC input plug (connected by the 10 wire ribbon cable). It is a cross cable! Color code valid for $V_{CC}(ADC)$ = black. Numbers within the plug-box are the pin-numbers of the plug. Labels *ADC_IN#* (# = 1…8) indicate input channel number # of ADC *LTC2308* [15]. *ADC_IN3* is ground for board revisions *Rev* ≤ 11.01.

Fig. 1.5 illustrates the pin assignment of the 10-pin ADC input plug (connected by the 10 wire ribbon cable seen in the photo). Numbers within the plug-box are the pin-numbers of the plug. Label *ADC_IN#* (# = 1…8) indicates input channel number # of the ADC *LTC2308* [15]. *ADC_IN3* is ground for board revisions *Rev* ≤ 11.01.

1.3 Outline

The organization of this communication is as follows:

Section 1	introduces into this document.
Section 2	offers some theoretical background.
Section 3	measures loop gains on the open loop.
Section 4	mesures loop gains on the closed loop using the *Middlebrook* method.
Section 5	compares and discusses the measured results achieved in chapters 3 and 4.
Section 6	draws conclusion and
Section 7	offers references.

2 Theoretical Backgrounds

Please read this Chapter 2 at home before coming to the practical training.

Do not spend your time in the lab with learning theoretical backgrounds!

Greyed out texts are optional. They explain the significance of the measurements for setting PID control parameters, but are not required for theis practical training.

2.1 Loop Model

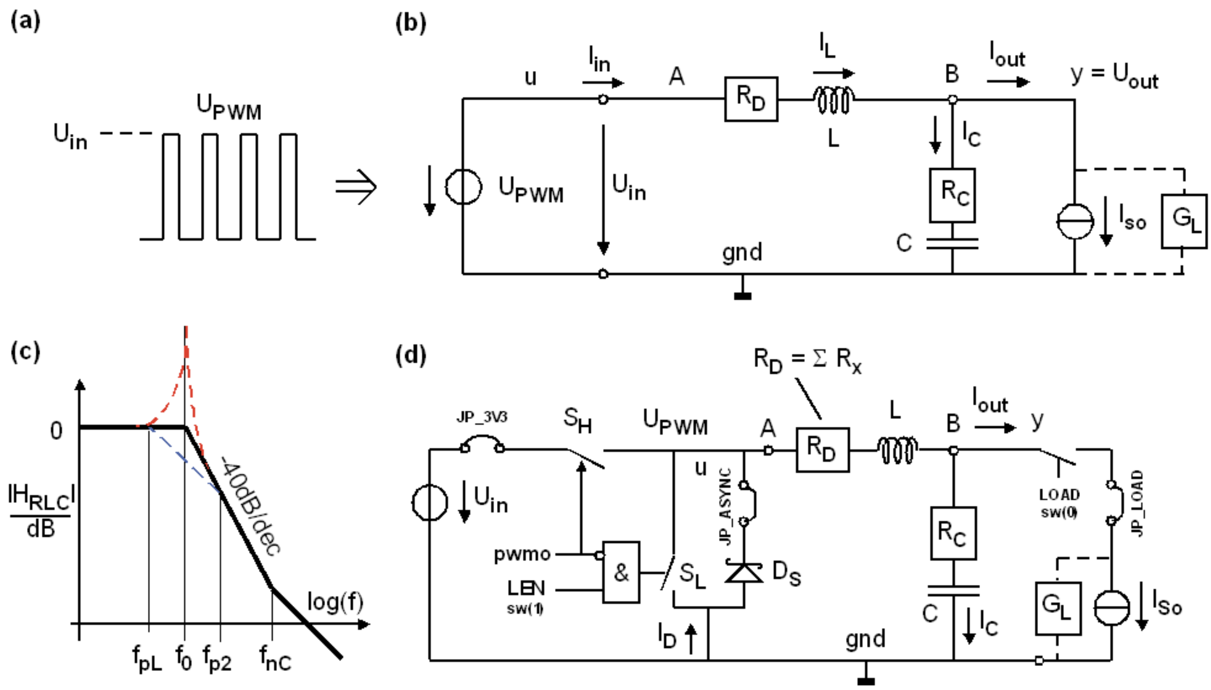
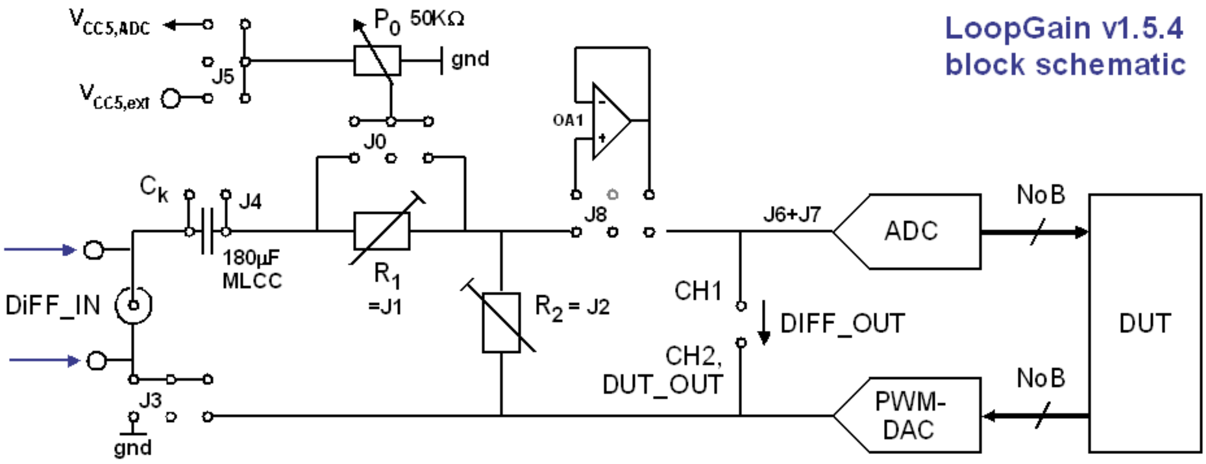


Fig. 2.1: *RLC* lowpass corresponding to boxes *Process* and *Inference* in Fig. 1.1
(a) PWM signal, **(b)** schematic with U_{PWM} generator, load current source I_{so} and its output conductance G_L, which is assumed to be negligible in this case, **(c)** amplitude diagram, **(d)** schematic illustrating generator switches and sync/async functionality of signal *LEN = LSE = sw(1)*.

2.2 Loop Gain Measurement Circuit

(a) *LoopGain R 1.5.4* board schematic block model



(b) *LoopGain R 1.5.4* boad detailed schematic model

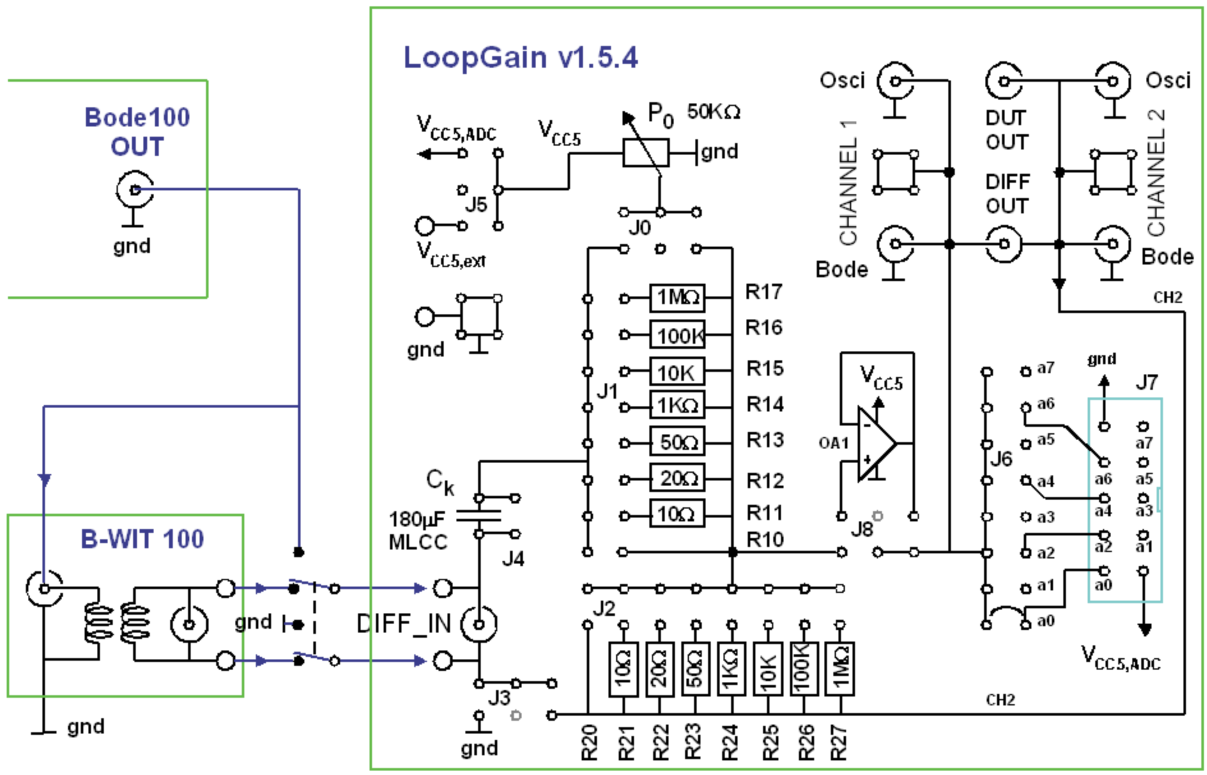


Fig. 2.2: *LoopGain R 1.5.4* board
(a) Schematic block model
(b) Detailed schematic model
(c) Eagle schematic (created by Huade Zhang)
(d) Eagle layout of created by Huade Zhang

Fig. 2.2 (c)
LoopGain R 1.5.4
Eagle schematic

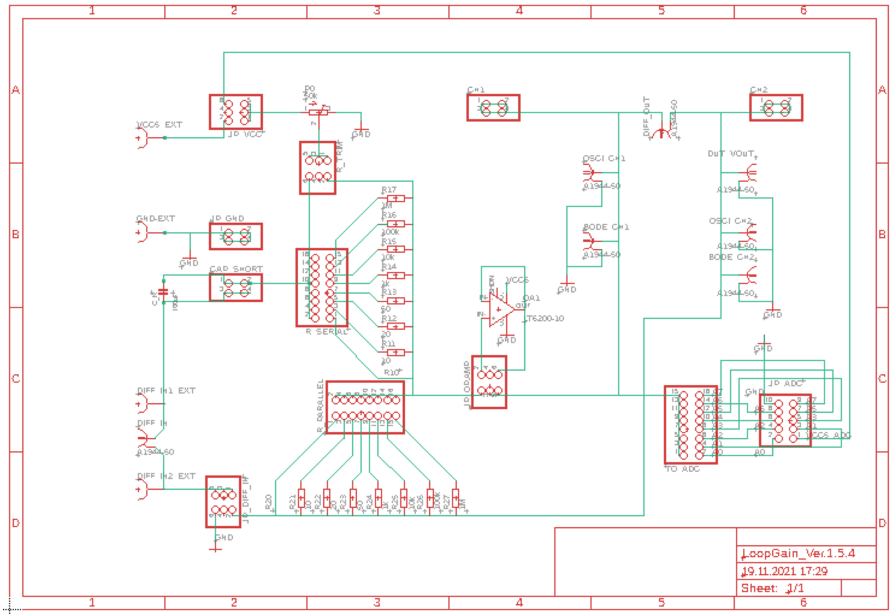
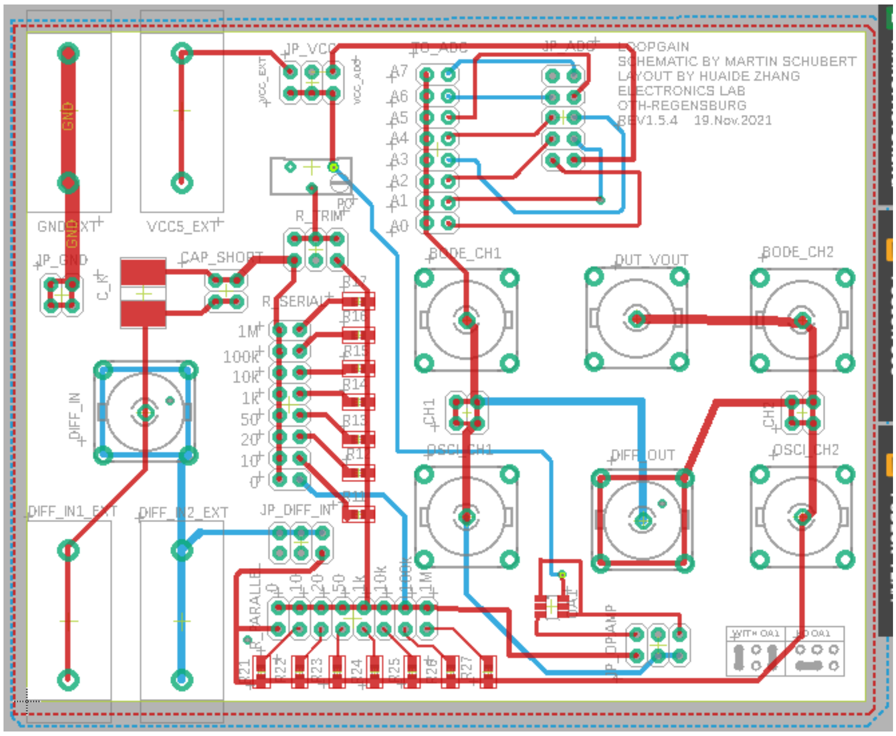


Fig. 2.2 (d)
LoopGain R 1.5.4
Eagle layout



2.3 Setting of Switches (sw) and Push Buttons (key)

Table 2.3: Functionality of switches *sw*(9:0) and push buttons *key*(3:0)

9	8	7	6	5	4	3	2	1	0
Set point (wanted) *w* in mV				DAC inp. sel		7seg inp. sel		LSE	i_{Load}

Switches	
sw(9:6)	Select set point *x* in V
0000	Set point w = 1250
0001	Set point w = 0
0010	Set point w = 250
0011	Set point w = 500
0100	Set point w = 750
0101	Set point w = 1000
0110	Set point w = 1500
0111	Set point w = 1650
1000	Set point w = 1750
1001	Set point w = 2000
1010	Set point w = 2250
1011	Set point w = 2500
1100	Set point w = 2750
1101	Set point w = 3000
1110	Set point w = 3300
1111	Set point w : defined by the *HPS**) using *Linux* program *set_w*; Set-point values out of range 2mV … Vin will be modified to 1234 mV. *) Hard Processor System, embedded in the FPGA
sw(5:4)	Select quantity fed to the input of the PWM DAC
00	control mode => output c
01	control mode => output v
10	control mode => output e
11	control mode => output w
sw(3:2)	Select quantity displayed on 7-segment display
00	display v in mV : label U -> output voltage
01	display w in mV : label i(nput) -> wanted output voltage
10	display i_L in mA : label L -> sampled inductor current
11	display i_{out} in mA : label o -> sampled output current
sw(1)	LSE: Low-side Switch Enable
0	Asynchronous mode: Low-side power-MOSFET is always off.
1	Synchronous mode: Low-side switch is ready to operate
sw(0)	Load current switch
0	Load current OFF
1	Load current of 1A ON

Keys	(=push buttons)
key(0)	Global asynchronous reset, dominant over all other signals: all flipflops are reset to their reset-states
key(1)	Global enable: flipflops do not change state when *key*(1) pushed
key(2)	Load current ON: pushing *key*(2) has the same effect as *sw*(0)='1'; current flow stops when *key*(2) is released.
key(3)	hold 7-segment display: 7seg-display frozen while *key*(3) pushed

Mini keys	(small push buttons), functionality according to [24].
left	HPS reset, restarts the hard processor system
middle	HPS User button, restarts the hard processor system
right	warm reset

2.4 Naming Scheme for Files Measured with *Bode100*

Table 2.4: Naming scheme of measured files required for plotting with *Matlab* program

Files 1), 2) within zip-file	method	chapter	Comment
Characterize_LoopGains_DCDCbuck.m		3, 4	*Matlab* script file
OL1_DCDCbuck_RLC.csv	3)	3.1	RLC only
OL2_DCDCbuck_ADC_RLC_DAC.csv	3)	3.2	*ADC + RLC + DAC*
OL3_DCDCbuck_Kp=1,Ki=Kd=0.csv	3)	3.3	*open loop,* $K_p=1$
OL4_DCDCbuck_Kp=10,Ki=Kd=0.csv	3)	3.4	*open loop,* $K_p=10$
OL5_DCDCbuck_Kp=100,Ki=Kd=0.csv	3)	3.5	*open loop,* $K_p=100$
MB3_DCDCbuck_Kp=1,Ki=Kd=0.csv	4)	4.3	closed loop, $K_p=1$
MB4_DCDCbuck_Kp=10,Ki=Kd=0.csv	4)	4.4	closed loop, $K_p=10$
MB5_DCDCbuck_Kp=100,Ki=Kd=0.csv	4)	4.5	closed loop, $K_p=100$
MB6_DCDCbuck_Kp=10,fix=1e3,Kd=0.csv	4)	4.6	cl. l., $K_p=10$, $K_i=2\pi f_{ix}$

1) To translate a file of type **.bode3* to a "comma-separated value" (csv) file, open a bode3 file in the *Bode Analyzer Suite*, select *File > Export > Field separator comma > Save as…*

2) Unzip the author's file *Characterize_LoopGains_DCDCbuck.zip* to find the listed files (filled with noise) and run the *Matlab* script *Characterize_LoopGains_DCDCbuck.m*.

3) *OL#* files are measured with the Open Loop technique used in section 4.

4) *MB#* files are measured with the Middlebrook technique presented in section 5.

Fig. 2.4 illustrates the target graphics to illustrate your measurements.

To make things work the file names must exactly match the file names listed in the table above, which are given in the zip file with same name.

The given data files contain noise. Replace them by your measurements.

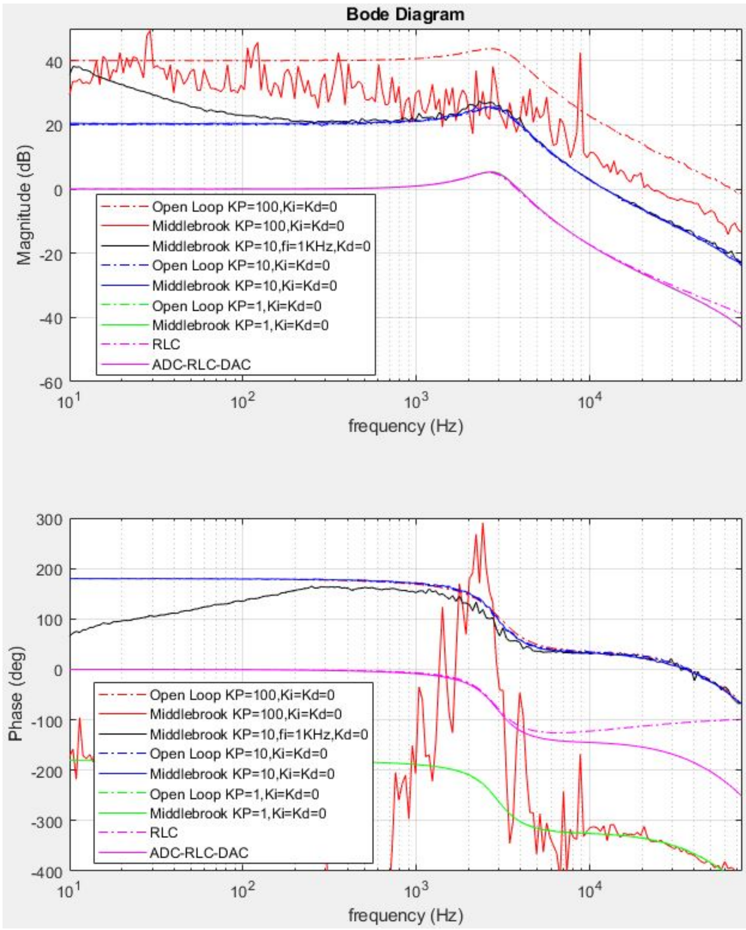


Fig. 2.4: Target graphics

2.5 Stability: Cross-Over Frequency f_x and Phase Margin Φ_M

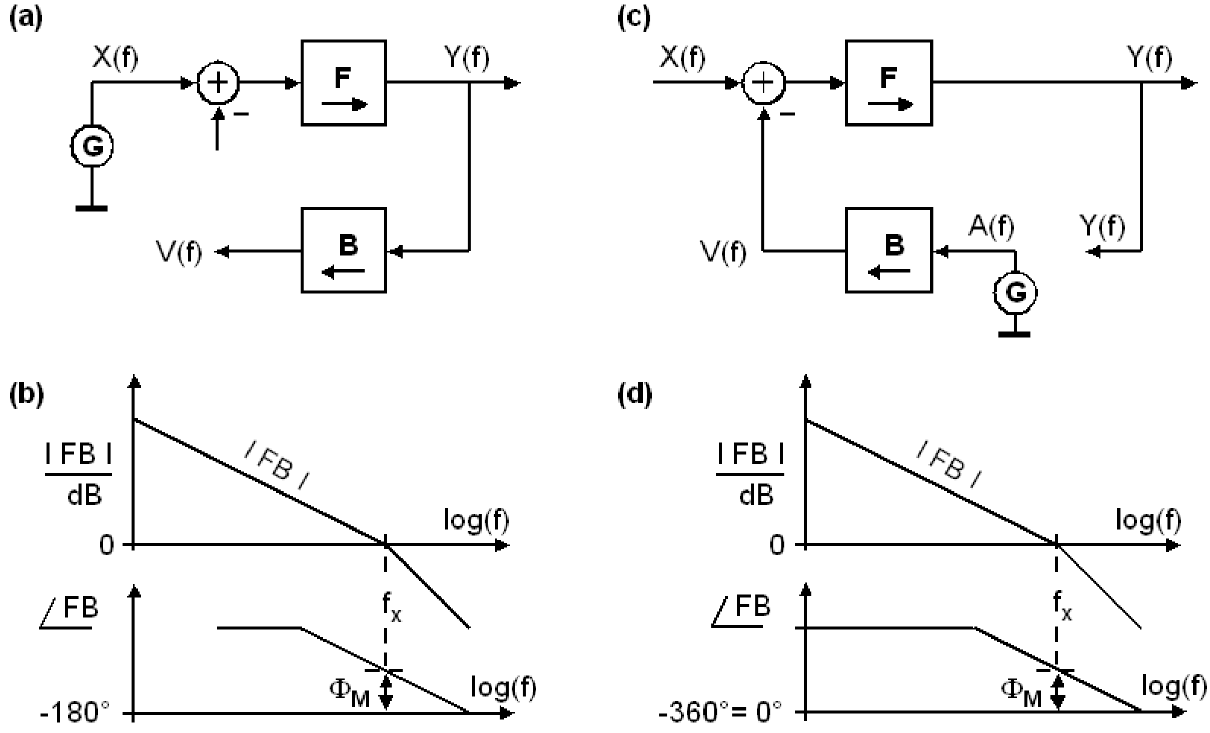


Fig. 2.5: Measurement of phase margin Φ_M of the (open) loop gain with (a) '-' sign excluded against (b) -180° and for (c) '-' sign included against (d) -360° = 0°.

The closed loop formula

$$STF = \frac{F}{1+F\cdot B} \xrightarrow{|FB|\to\infty} B^{-1}$$

with F and B being the total feed forward and feedback network, respectively, becomes an oscillator when the denominator becomes zero, i.e. when $FB = -1 = 1\cdot e^{-j180°}$.

Cross-over (or transit) frequency. The frequency where $|FB|$ becomes unity is said to be the cross over frequency f_x (or transit frequency f_T), i.e. $|FB(f_x)| = 1 = 0\text{dB}$.

The phase margin Φ_M is measured at f_x and is the phase distance from the harmonic oscillator. It should be $\Phi_M \geq 45°$. The 45° is measured

- versus -180° in the situation of Fig. 2.5(a), consequently $FB(f_x) = 1\cdot e^{j(-180°+\Phi_M)}$,
- versus -360° = 0° in the situation of Fig. 2.5(b), consequently $FB(f_x) = 1\cdot e^{j\Phi_M}$.

2.6 Background: Compensator Modeling

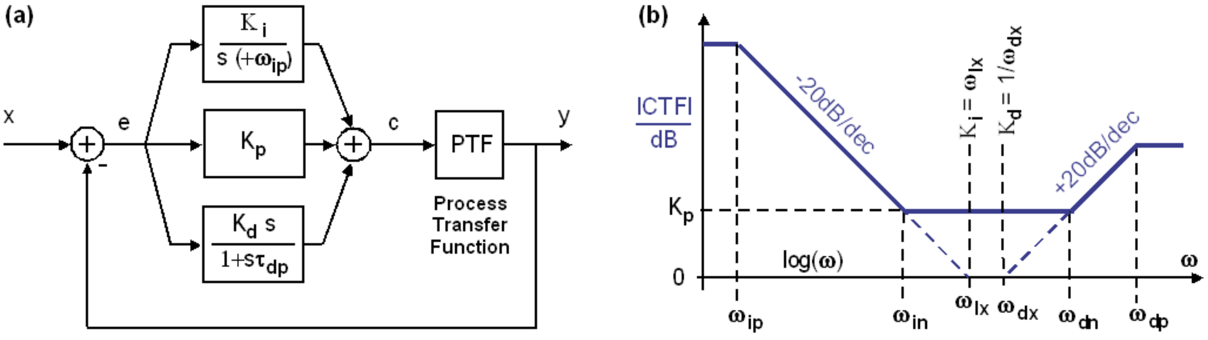


Fig. 2.6: Compensator design (a) Schematic block model and (b) Bode diagram

The control unit, also termed compensator as a microcontroller is a very wide broad term, is typically designed in the *PID* form, with *P* standing for proportional, *I* for integral and *D* for differential. The compensator transfer function is typically written in the form

$$CTF(s) = K_p + \frac{K_i}{s} + K_d \cdot s\,.$$

Frequently we find, that an additional differentiator pole is required for stability and an integrator pole is unavoidable, e.g. due to limited amplification, yielding

$$CTF(s) = K_p + \frac{K_i}{s+\omega_{ip}} + K_d \cdot \frac{s}{1+s\cdot\tau_{dp}} \qquad \text{with} \qquad \tau_{dp} = \frac{1}{\omega_{dp}}$$

with ω_{ip} being undesirable but unavoidable and typically not modeled except in *Spice*-like tools, where a tiny ω_{ip} is required to avoid divide-by-zero errors during DC or operating point computation. Using $\omega_{ip} = 0$ we can rewrite the compensator transfer function as

$$CTF(s) = K_P + \frac{\omega_{ix}}{s} + \frac{s}{\omega_{dx}} \cdot \frac{s}{1+s/\omega_{dp}}$$

to make the 0 dB crossover frequencies $\omega_{ix} = K_I$ and $\omega_{dx} = 1/K_D$ visible. Conclusion of

$$f_{ix} = \frac{\omega_{ix}}{2\pi} = \frac{K_i}{2\pi}\,,$$

$$f_{dx} = \frac{\omega_{dx}}{2\pi} = \frac{1}{2\pi\cdot K_d} \qquad \Leftrightarrow \qquad K_d = \frac{1}{\omega_{dx}}$$

$$f_{dp} = \frac{\omega_{dp}}{2\pi} = \frac{1}{2\pi\cdot\tau_{dp}}$$

is obvious. Furthermore, it is seen from Fig. 2.6(b) that we get the compensator transfer-function zeros

$$f_{in} = \frac{f_{ix}}{K_p} = \frac{\omega_{ix}}{2\pi K_p} = \frac{K_i}{2\pi K_p},$$

$$f_{dn} = f_{dx} \cdot K_p = \frac{\omega_{dx} \cdot K_p}{2\pi} = \frac{K_p}{2\pi \cdot K_d}.$$

3 Loop Gain Measurement with Open Loop

This is an introduction; practical work begins at Chapter 3.1!

Knowing loop-gain over frequency is a key information for optimal *P*, *PI* and *PID* control parameter setting. We shall try to measure loop gain on the open loop in this chapter.

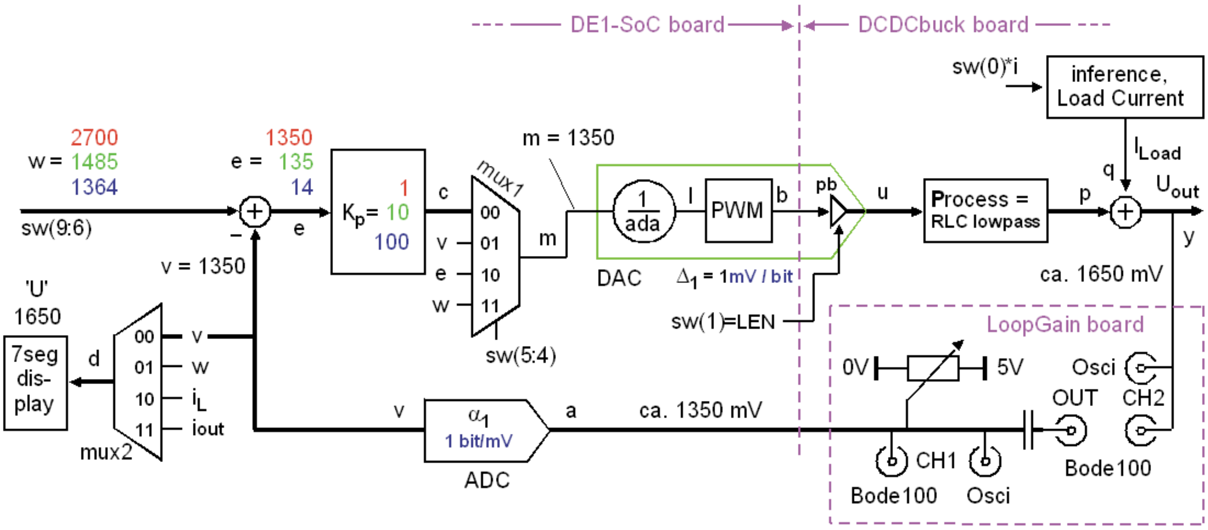


Fig. 3.0: General setup for open-loop gain measurement

General Remarks:

- Key importance: Check on the oscilloscope, that U_{out} delivers a sinusoidal signal!
- Set *Bode100's* receiver 1 and 2 attenuators such that the volume bars stay green and as big as possible, but never become red!
- The 7-segment display shows process variable *v*, the ADC output, indicated as 'U'.
- Set switches sw(9:6) such, that U_{out} oscillates ca. around 1350 mV.

Set input *w* according to Fig. 3.0

We want to have $U(a) = U_{ADCin} \cong$ 1350 mV and $m \cong U_{out} \cong$ 1350 mV. In Fig. 3.0 we see that $e = m / K_p$. to compute first the values for *e* required to achieve $K_p = \{1, 10, 100\}$. Compute in table 3.0 below the required setting voltage *w* to get for the different values of K_p Complete the fields in table 3.0 and …

Set the required values *w* with the embedded system. (If no embedded available, the nearest *w*).

Table 3.0: compute *e* and *w* for the different values of K_p.

K_p =	m =	e = m/K_p =	v =	w = v + e =	in section
1	1350	1350	1350	2700	3.3
10	1350	135	1350	1485	3.4
100	1350	13.5 → 14	1350	1364	3.5

Why do we need the LoopGain board (Nice to know)

The *LoopGain* board is necessary, because the *Bode100* cannot deliver a DC offset voltage: The capacitor following *Bode100's* output in Fig. 3.0 allows the potentiometer at its other terminal to build up a DC voltage on wire *a* (ADC input), labeled in Fig. 3.0 with 1350mV as ADC input operating point. To keep the impact of the DC-blocking capacitor out of the loop-gain measurement, *Bode100's OUT* and *CH1* input have to be separated in this exceptional case.

Why U_{out} = 1350 mV? (Nice to know)

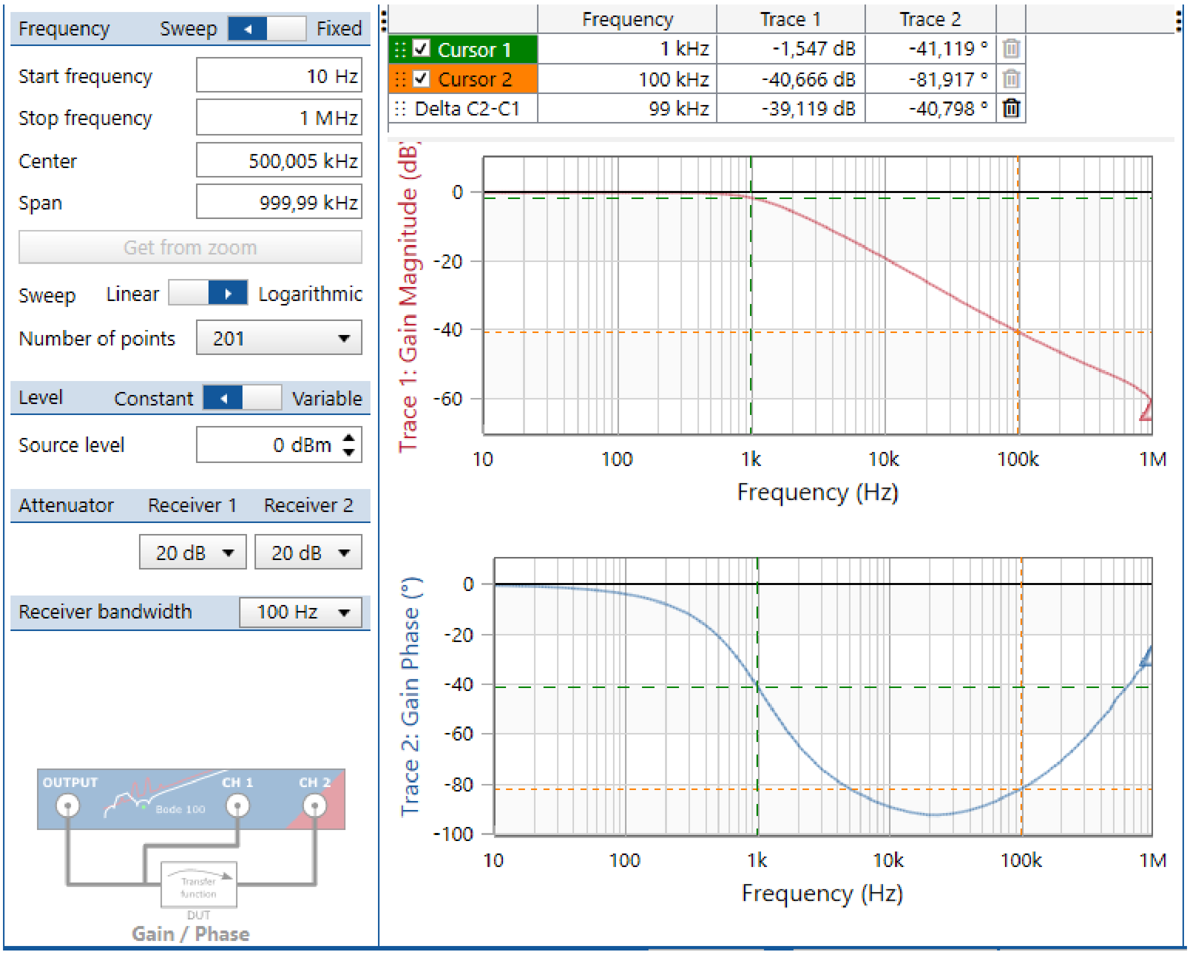
To operate the high-side switch of the PWM buffer amplifier, labeled *pb* in Fig. 3.0, the PWM signal must pulsate with minimum low- and high-level periods. Therefore, the maximum pulse width is limited by software to 270 of 330 PWM slots. Using U_{in} = 3.3V the maximum achievable average output voltage is $U_{out,max}$ = 2700 mV. The low-side switch can be operated for any U_{out}. Consequently, the center of the available output voltage range is $U_{out,mid}$ = (2700 mV – 0 mV)/2 = 1350 mV.

To do with *Matlab* during the following measurements

In the library *Models_ADA+DCDCbuck_edu* you will find in directory *Matlab* subdirectory *Characterize_LoopGains_DCDCbuck* provided by the author. It contains the *Matlab* script file *Characterize_LoopGains_DCDCbuck.m* and the 9 *.*csv* files listed in table 2.4.
Run the Matlab script file *Characterize_LoopGains_DCDCbuck.m* within the directory of the same name (extracted from the zip file with this name). *Matlab* should not deliver an error message, but a graphic containing noisy data delivered by the dummy *.*csv* files.
In the next chapters you will override the given noise files with your measured data to achieve meaningful loop-gain *Bode* plots

3.1 Measurement of the *RLC* Lowpass

(a) Transfer Function of the *RLC* lowpass (*PTF*) measurement with *Bode100*



(b) Measurement setup

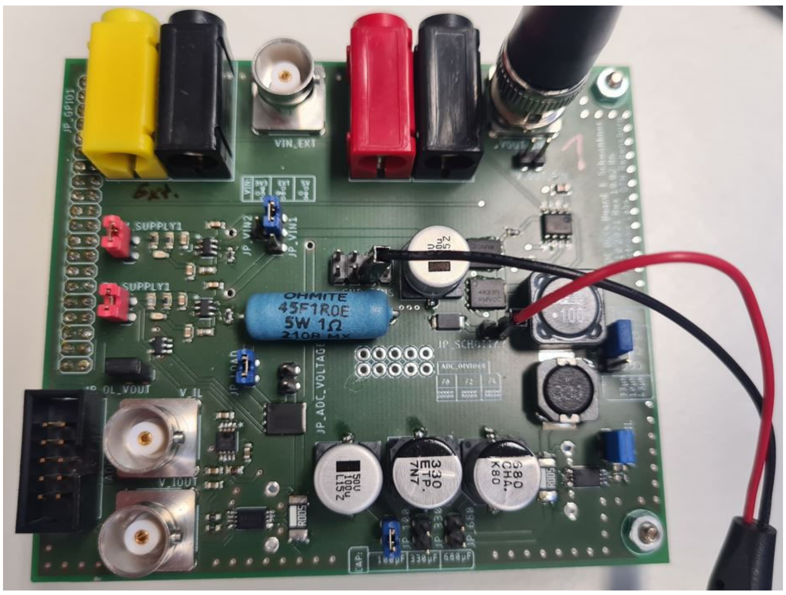


Fig 3.1: Characterization of the RLC lowpass of the *DCDCbuckR10* board

Detach the *DCDCbuck* board from the *DE1-SoC* board to be sure that all voltages are zero and both power-FETs driving the RLC lowpass are high impedant. Use the *Bode100 transmission* mode to get the transfer function of the RLC lowpass.

This lowpass transfer function corresponds to the *Plant* or *Process* of our control loop.

Fig 3.1 shows a measurement performed with *Bode100* of the *RLC* lowpass only with *DCDCbuck* board (Rev.5) being disconnected from any other device.

- Cursor 1 is at the position measured as f_0 in the impedance analysis above.
- Cursor 2 is near a zero at $f_n \approx 4$ KHz in the transfer function caused by R_C. That zero compensates for one of the double-poles (at 1KHz) for $f > f_n$. Consequently, attenuation for f >>10 KHz is 1st order only.

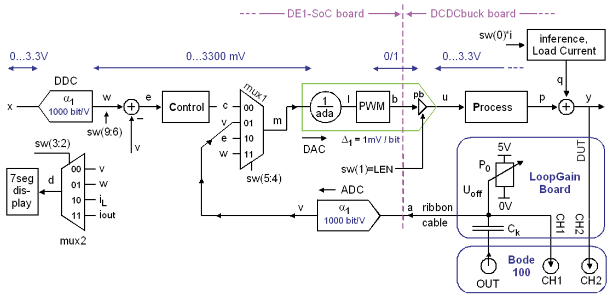
Measurements: Measure your own version of Fig. 3.1 for your individual *DCDCbuck* board. Save your *Bode100* measurement file as *OL1_DCDCbuck_RLC.bode3* and convert it to *OL1_DCDCbuck_RLC.csv*. You should be able to display it with the author's *Matlab* program *Characterize_LoopGains_DCDCbuck.m.*

Override the given noisy file with this name and view your measurement with *Matlab.*

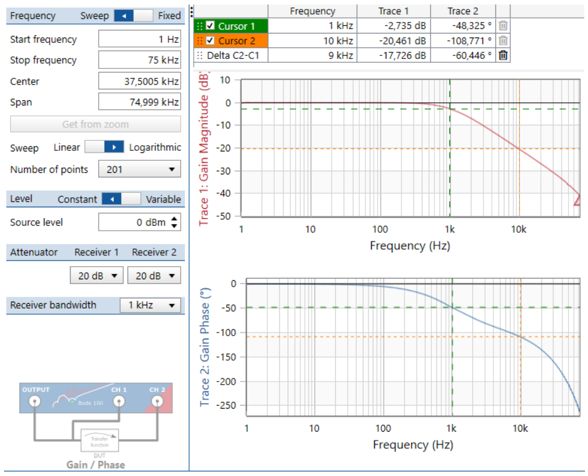
Using the *LoopGain* board in this practical guide, the connection from *Bode100's OUT*, labeled with "*Do not remove this cable*", must be exceptionally removed from *CH1*, so that this end of that *BNC* cable is hanging in the air.

3.2 Measurement of *ADC → RLC Lowpass → DAC*

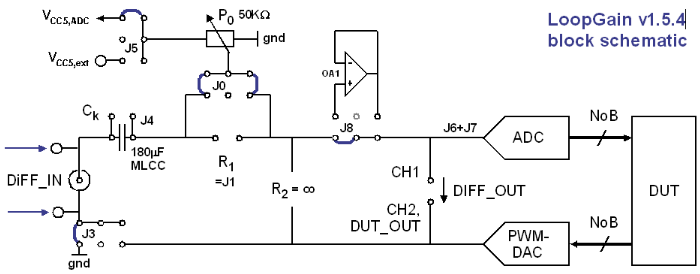
(a) Circuit to assemble (*mux2*-inputs *v, w, i_L, i_{out}* correspond to *c, v, e, w* , resp., of *DCDCbuck R5* board.)



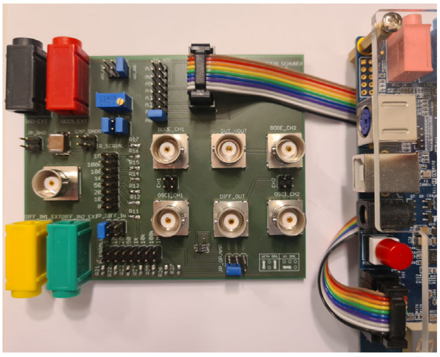
(b) Bode diagramm measured with *Bode 100*

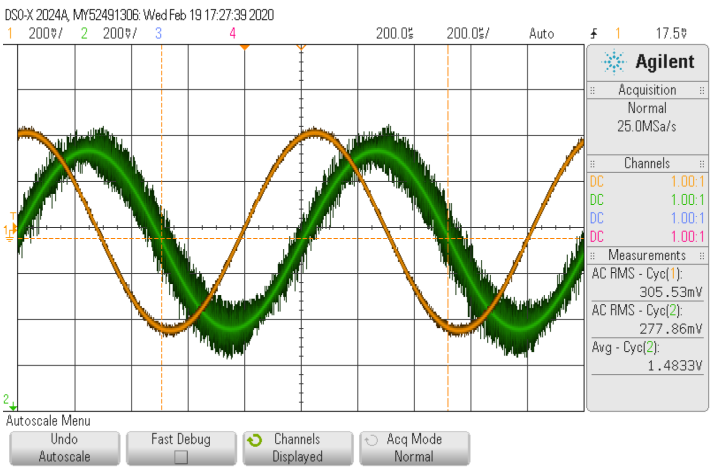


(c) *LoopGain* board block diagram



(d) Photo of *LoopGain* board plot the jumper settings in photo





(e) Oscillogram at $f = f_0 = 1$KHz.
Yellow: *CH1*, input at node *a*,
Green: *CH2*, output at node *y*.

Fig. 3.2: The DC/DC buck converter setup for the measurements of this chapter.

Measure the loop gain without compensator unit.

Use jumper settings for the *DCDCbuck* board as proven in document *Getting Started with DCDCbuck Board*. In this subsection, we will open the feedback loop by feeding the BNC output of the *DCDCbuck* board (Fig. part (a): label *y*) to the *LoopGain* board and use the 10-

wire ribbon cable to forward the signal to the ADC (Fig. part (a): label *a*), as illustrated in Fig. part (e). We will feed a voltage to the input of the ADC (label *a*) and observe its impact at output *y*, whereas in this case *y*=*p* as load current I_{out} = 0 and consequently *q*=0. Output *v* of the *ADC* is directly fed to the *PWM DAC*, achieved by setting *sw*(5:4) = "01". The 7-seg display will show the output of the ADC. Use *Quartus > Programmer* to program the *FPGA* with any given *ci_de1soc…Rev10_*.sof* files, e.g. *ci_de1soc_DCDCbuck_Rev10_KP=1,Ki=Kd=0.sof.*

Electrical Connections:

- Connect the *DCDCbuck* board to *DE1-SoC* board with *JP2*, the outer 40-pin plug.
- Set jumpers as illustrated in Fig. 3.2 (d), compare them with Fig. part (c).
- Connect the *LoopGain* board with 10-wire ribbon cable to the ADC input plug of the *DE1-SoC* board to get the *ADC's* V_{CC}=5V, *gnd* = 0V and connect to the ADC's input channel *A0*.
- Connect *LoopGain* board's plug labeled *DUT_*U_{OUT} to the output of your *DCDCbuck* board.
- Connect *LoopGain* board's plugs labeled "*Osci CH1*, *CH2"* to your osci. *CH1, CH2*, resp.
- Connect *LoopGain* board's plugs labeled "*Bode CH1*, *CH2*" to *Bode100's CH1*, *CH2*, resp.
- Connect *LoopGain* board's plug labeled "*DIFF_IN*" to *Bode100*'s *BNC* plug *OUTPUT*.
- Leave *LoopGain* board's *BNC* plug *DIFF_OUT* unconnected.

The DC value of *y* should closely follow *ADC* input *a*.

Set switches

Set sw(9:0)="xxxx **01** 00 1 0":

- *sw*(0)='0': no load current (We will use external current loads)
- *sw*(1)='1': synchronous, '0': asynchronous operation
- *sw* (3:2) = "00" : show *ADC* output *v* on the 7-segment display in mV.
- ***sw*(5:4)** = "**01**" : feed the ADC's output (*v* in Fig. 3.2) to the DAC.
- ***sw*(9:6)** sets *w*, the desired output voltage, which is irrelevant when *sw*(5:4) = "01".

Measurements: Turn poti P_0 on LoopGain board to add an offset to the AC output of *Bode100*, blocked by C_k . Observe the impact of poti P_0 on the 7-seg. display and turn it to ca. 1350mV

DC average voltage at point *y* of Fig. 3.2, from Oscilloscope: $U_{out}(y)$ = 1349 mV ....

DC offset voltage at point *a* of Fig. 3.2, 'U' from 7-seg display: $U_{off}(a)$ = 1350 mV ....

Use Bode 100 to measure a Bode diagram, frequency range 10 Hz … 75 KHz

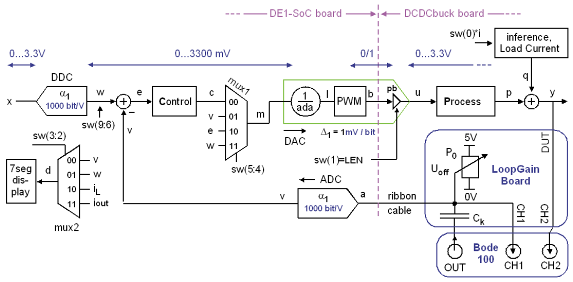
Bode100 output level: 0 dB, which corresponds to a peak-to-peak output voltage of 1.26V ....

Important: (A) Verify with an oscilloscope that measured curves are sinusoidal all time during recording with Bode100. Take your own *Bode* diagram with *Bode100* as shown in Fig. 3.2(b). (B) Set receiver 1 and 2 attenuations such, that their control bars are large but never red.

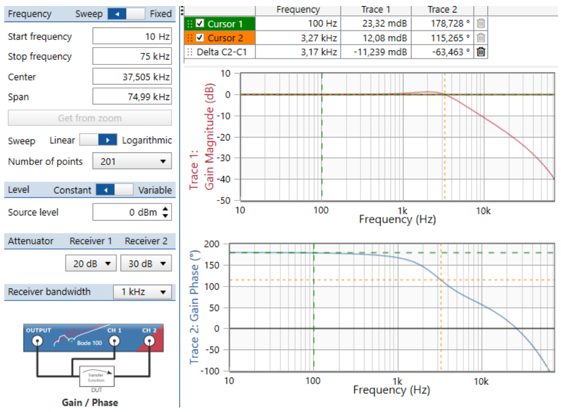
Save your *Bode100* measurement file as *OL2_DCDCbuck_ADC_RLC_DAC.bode3*. and convert it to *OL2_DCDCbuck_ADC_RLC_DAC.csv*. You should be able to display it with the author's *Matlab* program *plot_Bode100_data_from_csv.m*.

3.3 Include Compensator as Short Circuit $CTF(s) = K_p = 1$

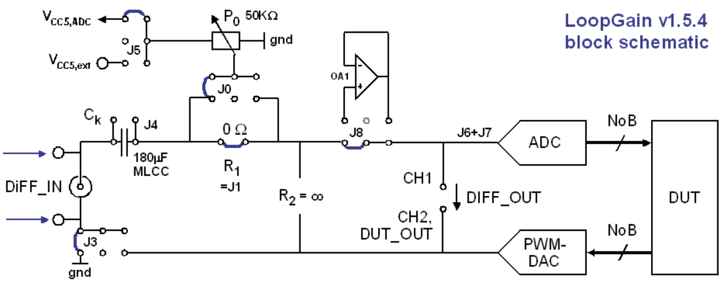
(a) Circuit to assemble (mux2-inputs v, w, i_L, i_{out} correspond to c, v, e, w , resp., for *DCDCbuck R5* board.)



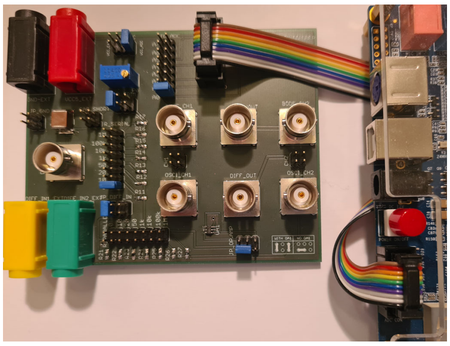
(b) Bode diagramm measured with *Bode 100*

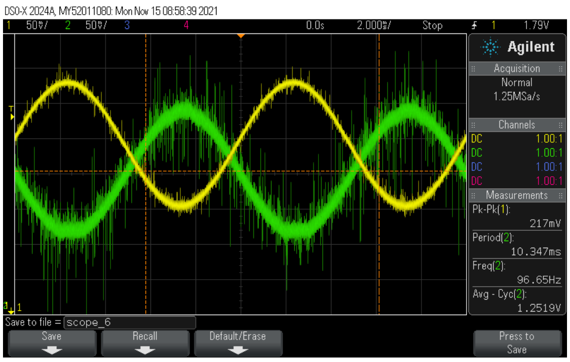


(c) *LoopGain* board block diagram



(d) Photo of *LoopGain* board plot the jumper settings in photo





(e) Oscillogram at f = 100 Hz.
Yellow: *CH1*, input at node *a*,
Green: *CH2*, output at node *y*.
Change observed: inversion.

Fig. 3.3: The DC/DC buck converter setup and measurements for the rest of this chapter.

Measure the loop gain with complete but open loop.

Feed a voltage to the input of the ADC (labeled *a*) and observe its impact at output *y*, whereas y=p as load current I_{out} = 0 and consequently q=0. Output *v* of the ADC is the feedback path of the control loop, which is achieved by setting *sw*(5:4) = "00".

Use the same electrical connections as in section 4.3, except jumper settings

- Set jumpers according to Fig. part (c), plot your settings in Fig. part(d)
- Connect the *LoopGain* board with 10-wire ribbon cable to the ADC input plug of the *DE1-SoC* board to get the *ADC's* V_{CC}=5V, gnd = 0V and connect to the ADC's input channel *A0*.
- Connect *LoopGain* board's *DUT_OUT* to the output of your *DCDCbuck* board.
- Connect *LoopGain* board's plugs labeled "*Osci CH1*, *CH2"* to your osci. *CH1, CH2*, resp.
- Connect *LoopGain* board's plugs labeled "*Bode CH1*, *CH2*" to *Bode100's CH1*, *CH2*, resp.
- Connect *LoopGain* board's plug labeled "*DIFF_IN*" to *Bode100*'s *BNC* plug *OUTPUT*.
- Leave *LoopGain* board's *BNC* plug *DIFF_OUT* unconnected.

Set switches *sw*(9:0)

We will now include the controller into the loop by setting *sw*(5:4)="00".

Set switches

Set sw(9:0)="1100 **00** 00 1 0"
sw(0)='0': no load current (We will use external current loads)
sw(1)='1': synchronous operation
sw (3:2) = "00" : show *ADC* output *v* on the 7-segment display in mV.
***sw*(5:4)** = "**00**" : feed the controller output (*c* in Fig. 3.2) to the *DAC*.
***sw*(9:6)** ="1100" selects *w*, here 2750 mV. We will get $y = w - v$ in mV.

Programming the compensator

Program the FPGA with a controller corresponding to a short: *CTF*(*s*) = 1.
(Use *Quartus* to program the *FPGA* with *ci_de1soc_DCDCbuck_Rev10_KP=1,Ki=Kd=0.sof*.)

Measurements

Turn poti P_0 such, that DC average output voltage of the *DCDCbuck* is $y = U_{in}/2 = 1.35$V. Observe the corresponding *ADC* input voltage at node *a* on the 7-segment.

DC average voltage at point ***y*** of Fig. 3.3(a), from Oscilloscope: $U_{out}(y)$ = **1350 mV** . . . .

DC offset voltage at point ***a*** of Fig. 3.3(a), 'U' from 7-seg display: $U_{off}(a)$ = **1356 mV** . . . .

Use Bode 100 to measure a Bode diagram, frequency range 10 Hz … 75 KHz

Set Bode100 output level to 0 dB, corresponding to peak-to-peak output voltage of **1.26V** . . . .

Verify with an oscilloscope that curves are sinusoidal. Take a *Bode* diagram with *Bode100* as shown in Fig. 3.3(b). This Bode diagram should be very similar to that in Fig. 3.2, except...

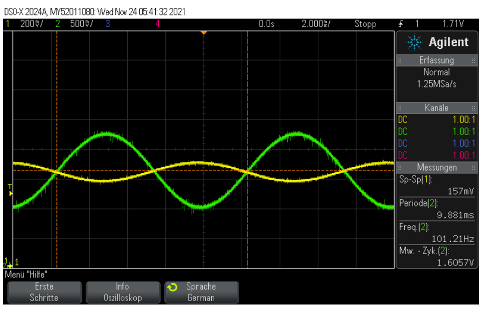
180° phase shift ⇔ inversion of the AC signal
. . . .

Save your *Bode100* measurement file as *OL3_DCDCbuck_Kp=1,Ki=Kd=0.bode3*. and convert it to *OL3_DCDCbuck_Kp=1,Ki=Kd=0.csv*. You should be able to display it with the author's *Matlab* program *plot_Bode100_data_from_csv.m*.

3.4 Compensator is a Constant Amplifier $CTF(s) = K_p = 10$

Use the same settings as in section 3.3, with exception of a compensator amplification of $CTF(s) = K_p = 10$ programmed within the *FPGA*. (Use *Quartus* to program the *FPGA* with *ci_de1soc_DCDCbuck_Rev10_KP=10,Ki=Kd=0.sof*.) As the AC input voltage a point ***a*** is now amplified by 20 dB, the *Bode100* output signal must be attenuated by the same amount.

(a) Oscillogram at f = 100 Hz. curves must be sinuoidal! Yellow: *CH1*, input at node *a*, Green: *CH2*, output at node *y*



(b) Bode diagramm measured with *Bode 100*

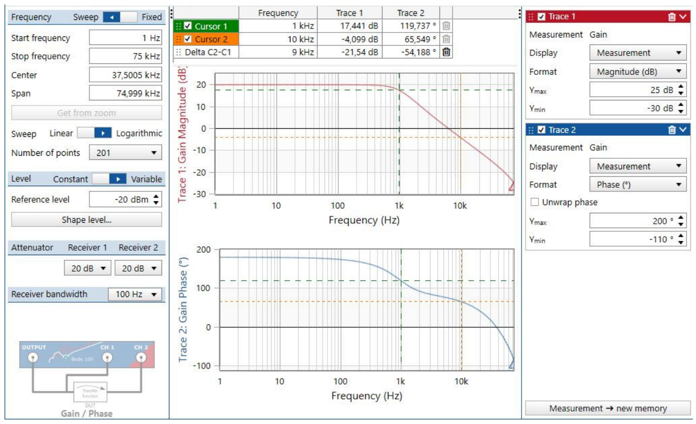


Fig. 3.4: The DC/DC buck converter measurements of this chapter.

Measurements

Turn poti P_0 such, that DC average output voltage of the *DCDCbuck* is $y = U_{in}/2 = 1.35$V. Observe the corresponding *ADC* input voltage at node *a* as *v* on the 7-segment. Take care, that both curves on the oscilloscope are sinusoidal.

DC average voltage at point *y* of Fig. 3.3(a), from Oscilloscope: $U_{out}(y)$ = 1352 mV . . . .

DC offset voltage at point *a* of Fig. 3.3(a), 'U' from 7-seg display: $U_{off}(a)$ = 1286 mV . . . .

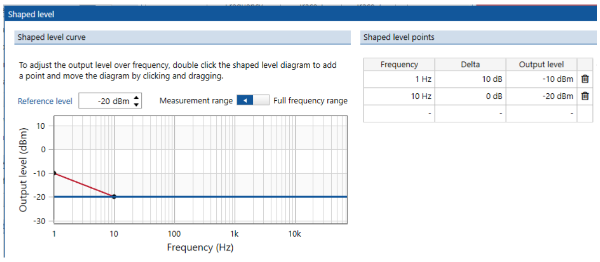
Use Bode 100 to measure a Bode diagram, frequency range 10 Hz … 75 KHz

Bode100 output level -20 dB, corresponding to peak-to-peak output voltage of 126mV . . . .

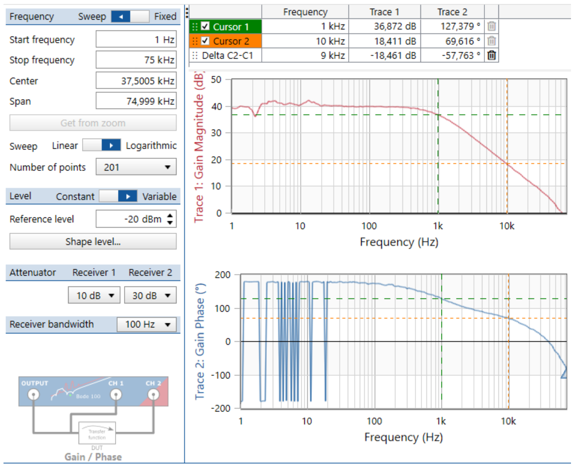
Save your *Bode100* measurement file as *OL4_DCDCbuck_Kp=10,Ki=Kd=0.bode3*. and convert it to *OL4_DCDCbuck_Kp=10,Ki=Kd=0.csv*. You should be able to display it with the author's *Matlab* program *plot_Bode100_data_from_csv.m*.

3.5 Compensator is a Constant Amplifier $CTF(s) = K_p = 100$

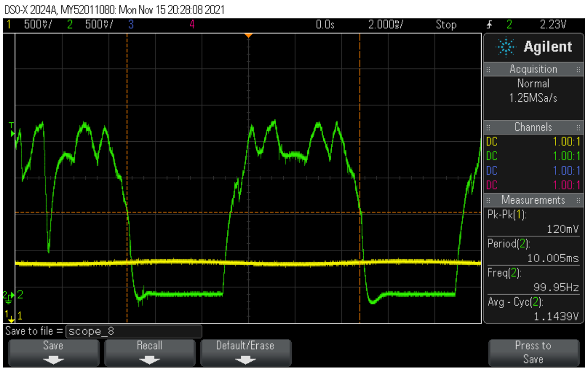
(a) Oscillogram at f = 100 Hz.
curves must be sinuoidal!
Yellow: *CH1*, input at node *a*,
Green: *CH2*, output at node *y*



(b) Bode diagramm measured with *Bode100*



(b) Oscillogram at f = 100 Hz,
Bode100 source level -30dB, without attenuator, curves must be sinuoidal !
ye: *CH1* @ node *a*, green *CH2* @ node *y*.



(c) Oscillogram at f = 100 Hz, *Bode100* source level -36…-40dB (using a BNC attenuator). Yellow: *CH1* @ node *a*, green: *CH2* @ node *y*.

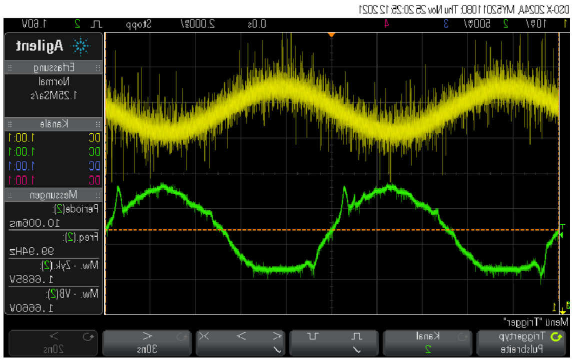


Fig. 3.5: Measurements at DCDCbuck board with $CTF(s) = K_P = 100$.

Measurements

Use *Quartus*, program the *FPGA* with *ci_de1soc_DCDCbuck_Rev10_KP=100,Ki=Kd=0.sof*. Turn poti P_0 such, that DC average output voltage of the *DCDCbuck* is $y = U_{in}/2 = 1.35$V. Observe the corresponding *ADC* input voltage at node *a* on the 7-segment.

DC average voltage at point *y* of Fig. 3.3(a), from Oscilloscope: $U_{out}(y)$ = 1366 mV
. . . .

DC offset voltage at point *a* of Fig. 3.3(a), 'U' from 7-seg display: $U_{off}(a)$ = 1339 mV
. . . .

Use Bode 100 to measure a Bode diagram, frequency range 10 Hz … 75 KHz.
Use a 20 dB attenuator to get the curve into the near sinusoidal shape as shown in Fig. 3.5(b).
Verify it at a constant frequency of 100 Hz.

Save your *Bode100* measurement file as *OL5_DCDCbuck_Kp=100,Ki=Kd=0.bode3*. and convert it to *OL5_DCDCbuck_Kp=100,Ki=Kd=0.csv*. You should be able to display it with the author's *Matlab* program *plot_Bode100_data_from_csv.m*.

3.6 Compensator Contains an Integrator: $CTF(s)=K_p=1, f_i=1$ KHz

(Use *Quartus* to program *FPGA* with *ci_de1soc_DCDCbuck_Rev10_KP=1,fi=1e3,Kd=0.sof*.)

Measurements

Turn poti P_0 such, that DC average output voltage of the *DCDCbuck* is $y = U_{in}/2 = 1.35$V. Observe the corresponding *ADC* input voltage at node *a* on the 7-segment.

DC average voltage at point *y* of Fig. 3.3(a), from Oscilloscope: $U_{out}(y)$ = **xxxx** . . . .

DC offset voltage at point *a* of Fig. 3.3(a), 'U' from 7-seg display: $U_{off}(a)$ = **xxxx** . . . .

Describe the problem of open loop measurements with high DC gain:

Due to the high DC gain of the integrator we cannot torn poti P0 such, that y comes close to 1.35V. It is either at its minimum level close to 0V or at its maximaum level of 2.75V (Higher levels are prohibited by software, as the charge pump of the LM27222 power-FET driver chip needs that U(SW) toggles up and down.