Design, Manufacturing, Optimization and Characterization of a DC/DC Buck Converter Board Driving Up to 30V/4.5A for FPGA and µC Control

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February 2019

ABSTRACT

Switching mode DC/DC converter had became critical building block in a portable devices nowadays. Research on digital control of the DC/DC converter had been conducted widely in order to compete with the analog control which had been used for long time. In this thesis, the design of the DC/DC Buck Converter is the main focus in order to provide a platform for further research on the digital control in both FPGA and microcontroller. The design of DC/DC buck converter is done by using LM27222 MOSFET driver to drive the FETs with LC lowpass filter. It is designed to be plugged in DE1-SoC Board from Terasic and also can be interfaced to any microcontroller board. STM32 microcontroller is used as proof of concept in this thesis. The buck converter can be operated in both synchronous and asynchronous mode by controlling the LEN flag. At the same time, the output is controlled by digital PWM pin. Detailed documentation on the DC/DC Buck Converter will be presented in this thesis including the design consideration, design schematic, board layout as well as output results. Further work can be done with this board such as software optimization in the digital control in order to investigate the performance of microcontroller and FPGA and etc..

Keywords: DC/DC converters, Buck Converter, Pulse Width Modulator (PWM), Digital Control

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LIST OF ABBREVIATIONS

AC	Alternating Current
CCM	Continuous Conduction Mode
DC	Direct Current
DCM	Discontinuous Conduction Mode
FET	Field Effect Transistor
FPGA	Field Gate Programmable Array
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
μC	Microcontroller

CHAPTER 1

INTRODUCTION

1.1 Introduction

DC/DC power converter had been widely used in most of the industrial and residential applications such as fuel cells, photovoltaic sources, electronics power supplies and many others. DC/DC converter had shown us both the fast speed and the capability of managing high power if needed. It had been used in processing more than 90% of the total amount of energy generated before its final consumption in this world nowadays [1].

DC/DC Buck Converter supplies a lower voltage than the input voltage. It is one of the most widely used power converters. As the output of the DC/DC buck converter is directly affected by the input voltage and the output current, a feedback control loop is necessary. It results in the underlying topology of buck converter is non-smooth as it switches back and forth according to the control signal in order to maintain the output voltage. There are various control techniques applied to the buck converter nowadays. More research and investigation is still carried on in order to improve its performance.

However, before any testing on the control method for a power converter, a reliable and robust design of DC/DC buck converter plays an important role. In this thesis, the design, optimization and the characterization of DC/DC buck converter will be discussed in details.

1.2 Problem Statement

Nowadays, the conventional sources of energy are depleting and the demand for the supply is increasing at a very rapid rate. Therefore, renewable energy such as wind and solar energy have been blooming up lately. However, the problems associated with the use of these energy sources and the output generated is not constant as it is dependent on the weather condition. Moreover, the output generated is DC output. Therefore, DC/DC buck converter is used to stabilize the output voltage from a range of input voltage with the most common switching control techniques which are PWM with high efficiency.

Digital control of the DC/DC converter had been implemented widely nowadays. With the advantages shown by the digital control [3][5] especially with ADC available, it is great to show the digital control comparison by both microcontroller and FPGA. Therefore, a DC/DC buck converter is required as the main element in the research.

1.3 Aim of the Study

The aim of the study is to design, optimize, manufacture and characterize the DC/DC Buck Converter PCB Board for FPGA and microcontrollers control in future.

1.4 Outline of the Report

The whole thesis will mainly focus on the DC/DC buck converter board design and its characterization. Chapter 1 of the thesis is mainly discuss on the introduction and the purposes of the study.

Chapter 2 will mainly attach the design schematic and PCB board design layout for the DC/DC buck converter designed throughout the period of conducting this thesis.

Chapter 3 will mainly discuss on the design schematic part by part in details.

Chapter 4 will mainly highlight on the design consideration. The characterization and optimization of the design which includes the inductor selection and the effect of external gate resistance for both high side FET and low side FET will be presented.

Chapter 5 will discuss on the results obtained including the inductor current and the output voltage at both loaded and unloaded condition.

Chapter 6 will conclude the whole thesis and provide some recommendations for further work.

CHAPTER 2

DESIGN SCHEMATIC AND BOARD LAYOUT

2.1 Design Schematic of DC/DC Buck Converter

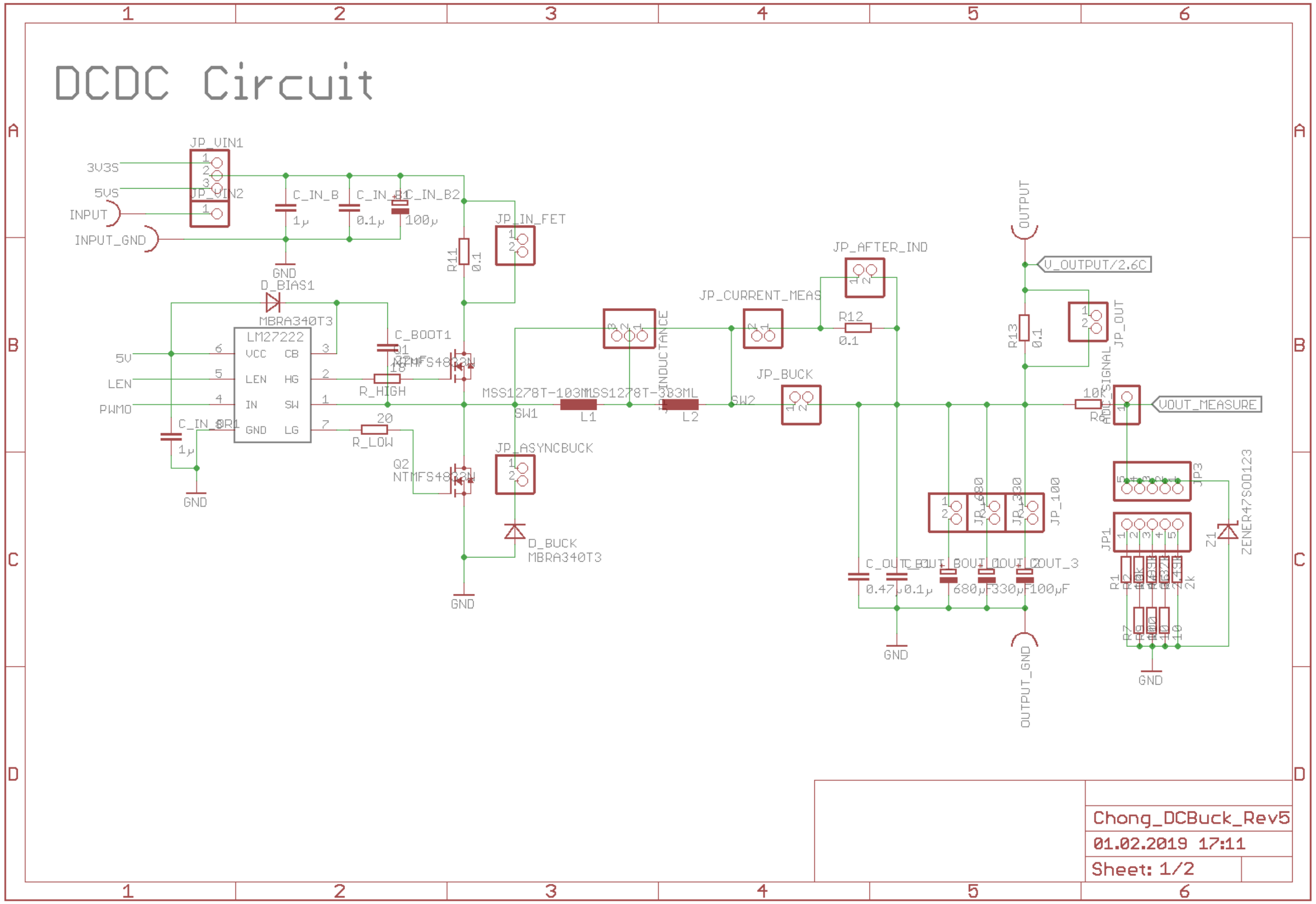


Figure 2.1: Design Schematic (Sheet 1/2)

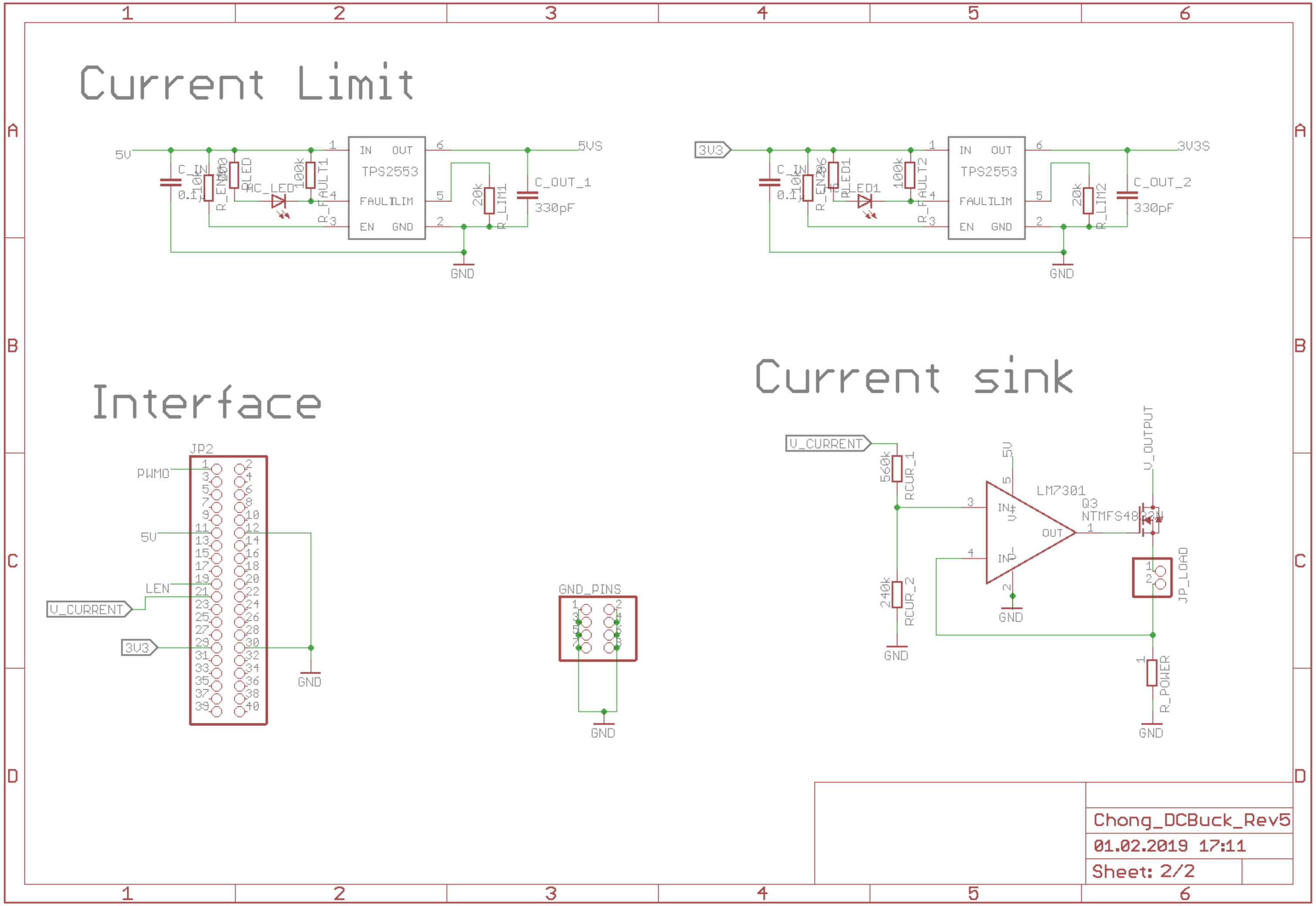


Figure 2.2: Design Schematic (Sheet 2/2)

2.2 Board Layout of DC/DC Buck Converter

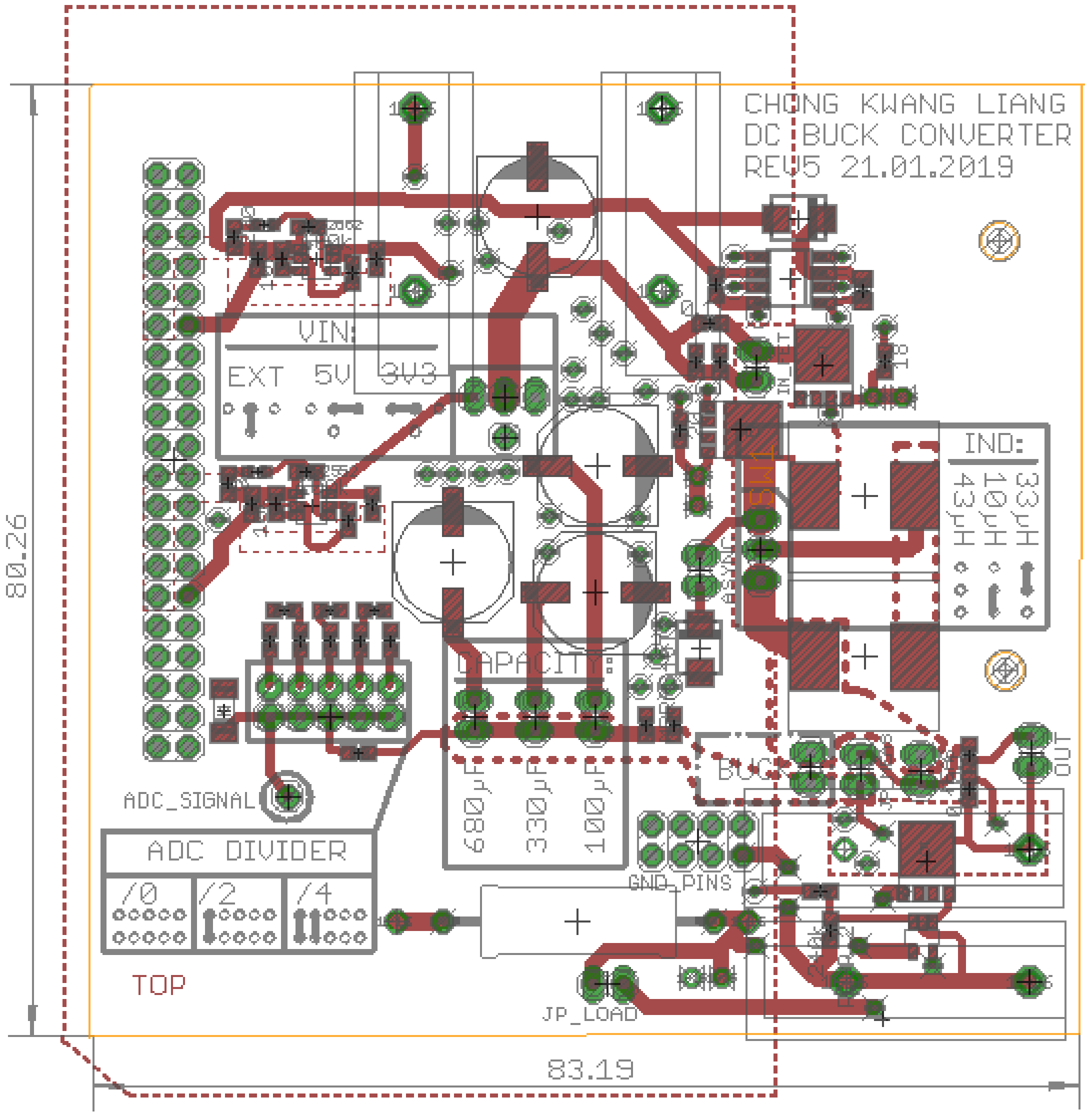


Figure 2.3: Top View of the Board Layout

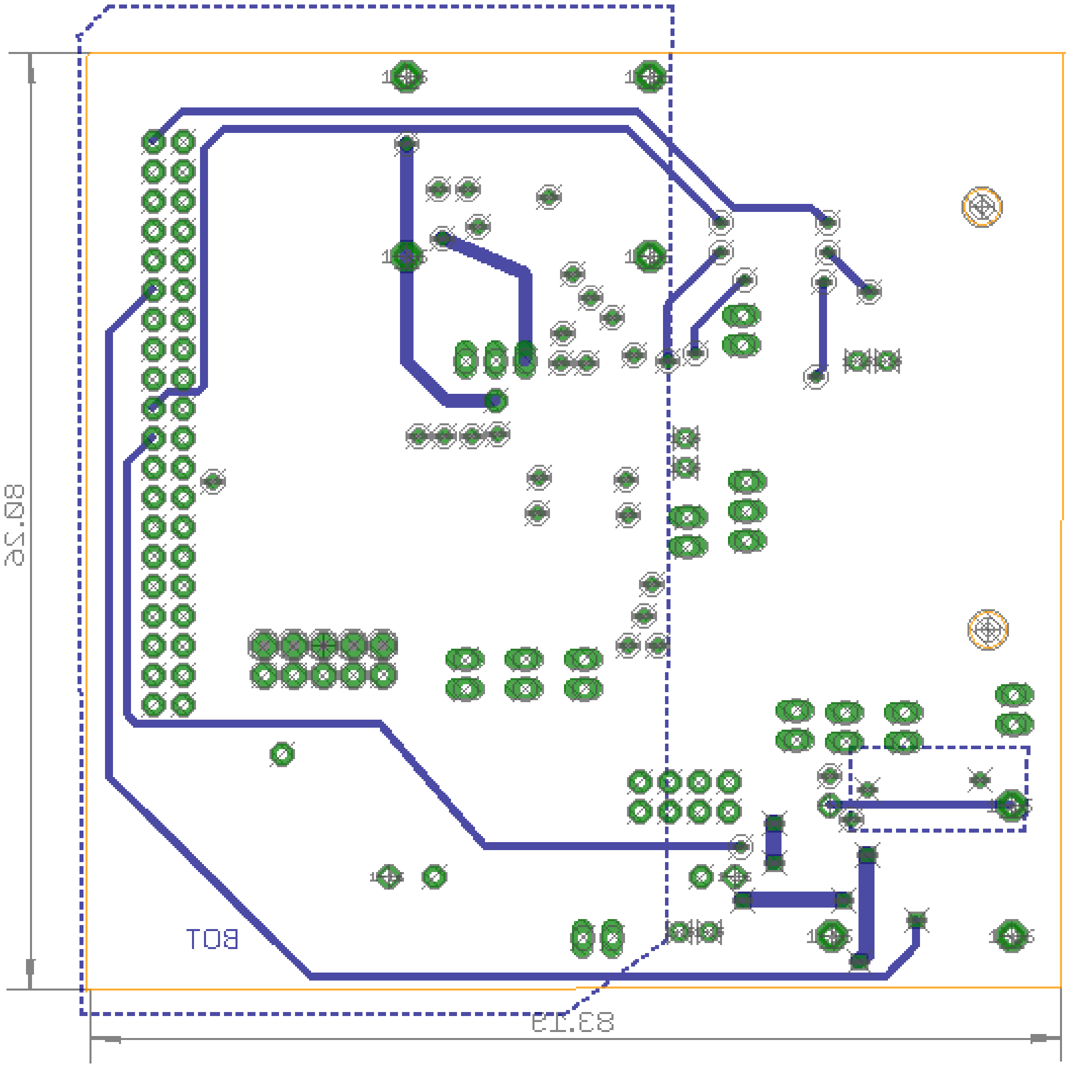


Figure 2.4: Bottom View of the Board Layout

CHAPTER 3

DESIGN ANALYSIS

3.1 Analysis of DC/DC Board Converter

3.1.1 FETs Switching

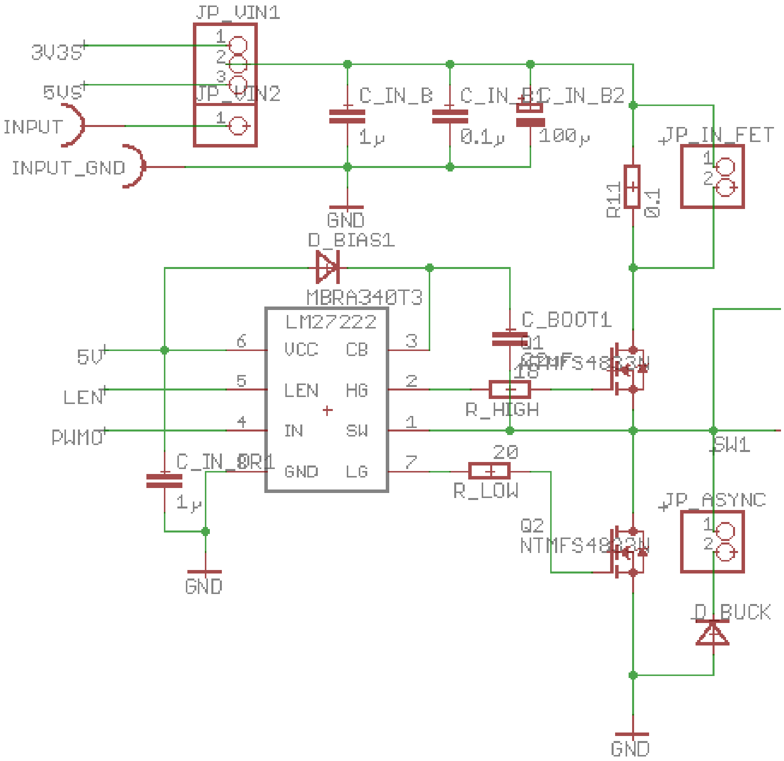


Figure 3.1: Switching of FETs

The switching of FETs is performed by LM27222 chip. LM27222 is a dual N-channel MOSFET driver which is designed to drive MOSFETs in push pull configuration. It takes the PWM output from controller and provides the proper timing and power level to MOSFETs. The high side FET will operate synchronously with the PWM signal while the low side FET will work inversely to it.

The bootstrap capacitor is connected from the supply rail to the output of the LM27222-circuit (SW) in order to generate high voltage at source pin of high side FET. It is done so in order for the use of direct gate drive circuits for the high side N channel MOSFET.

3.1.2 Current Limiter Circuit

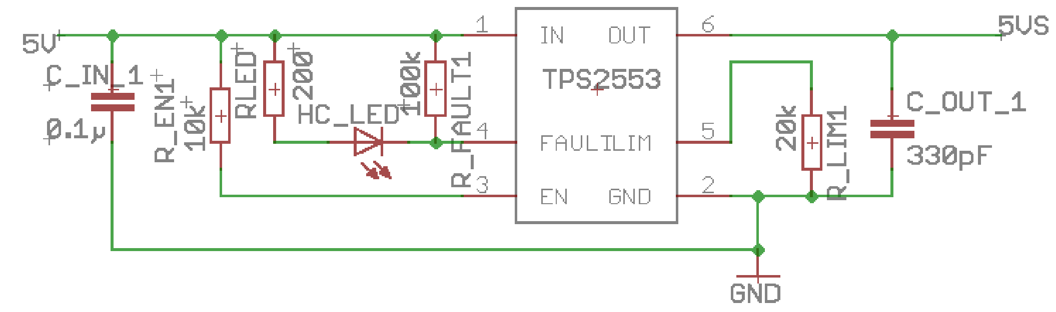


Figure 3.2: 5V Current Limiter Circuit

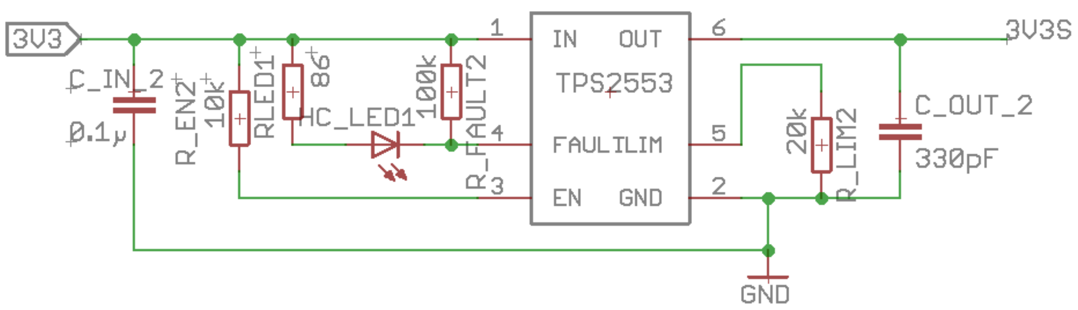


Figure 3.3: 3.3V Current Limiter Circuit

Figure 3.2 and Figure 3.3 above show the current limiter circuit for 5V and 3.3V respectively. The current limiter circuit is designed by using TPS2553 power distribution switch. It is able to provide up to 1.5A continuous load current. At the same time, the current limiter threshold can be adjusted from 75mA up to 1.7A via external resistor which is connected to ILIM pin (pin 5).

In both 5V and 3.3V current limiter circuit, the R_{ILIM} is selected at 20kΩ. Therefore, the typical current limit is calculated according to datasheet as below:

$$I_{osnom}(mA) = \frac{23950V}{{R_{ILM}}^{0.977} k\Omega} = 1283\ mA$$

3.1.3 Current Sink Circuit

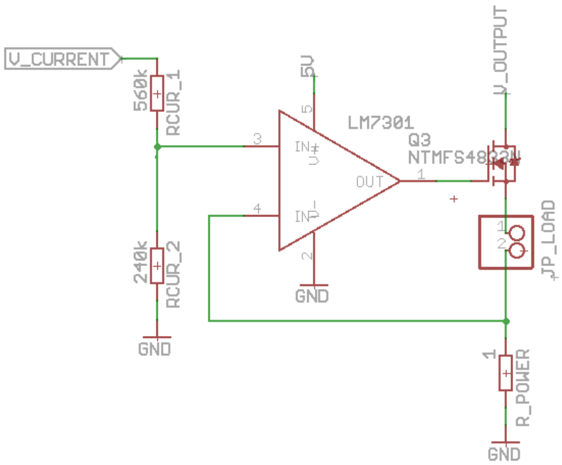


Figure 3.4: Schematic of Current Sink Circuit

Figure 3.4 above shows the current sink circuit which is implemented on the DC/DC Buck Converter Board. The control pin, $V_{CURRENT}$ is connected to either microcontroller or FPGA in order to connect or disconnect the load from the circuit. When $V_{CURRENT}$ pin is set to HIGH, there will be approximately 1V due to the voltage divider at the non-inverting terminal of the op-amp. Thus, it will switch on the power FET which allow the current to flow through the power resistor. The current flowing through the power resistor will be approximately 1A when jumper JP_LOAD is set, otherwise 0A.

3.1.4 ADC Divider

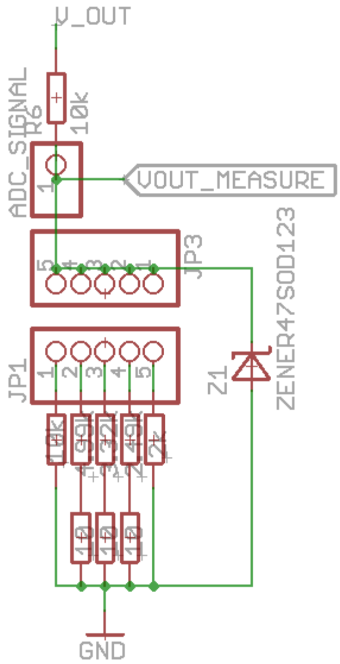


Figure 3.5: ADC Divider Circuit

ADC divider circuit is a simple potential divider circuit. There are number of jumpers for user to select the factor of divider in steps of factor two from 2 to 10 respectively. The zener diode is connected to protect the ADC input against overvoltages over 5V.

3.2 Features of DC/DC Circuit

For the DC/DC Buck Converter that is designed, there are a few control parameters. Firstly, the DC/DC Buck Converter can be operated in either synchronous or asynchronous mode through the selection on LEN pin (pin 19). LEN pin is low side FET enable pin which will start or stop the switching of low side FET. The converter will be operated in the asynchronous mode if the LEN pin is LOW and vice versa. On the other hand, the jumper for the Schottky diode can be connected in order for providing a return path during asynchronous operation, else internal diode of FET which has the greater voltage loss will be operated.

Moreover, there is a current sink circuit which is designed in order for the load to draw approximately 1A load current. The selection can be done by setting the pin V_CURRENT (pin 21) to HIGH.

CHAPTER 4

DESIGN CONSIDERATION

4.1 Inductors Selection

In the design schematic which in attached in previous chapter, 43µH inductor was chosen for the design with the series of 33µH and 10µH inductors. Jumper was designed in between the inductors in order for the user to short either inductor if necessary. The inductors were selected based on the simulation result of Power Stage Designer Tool by Texas Instruments. [6]

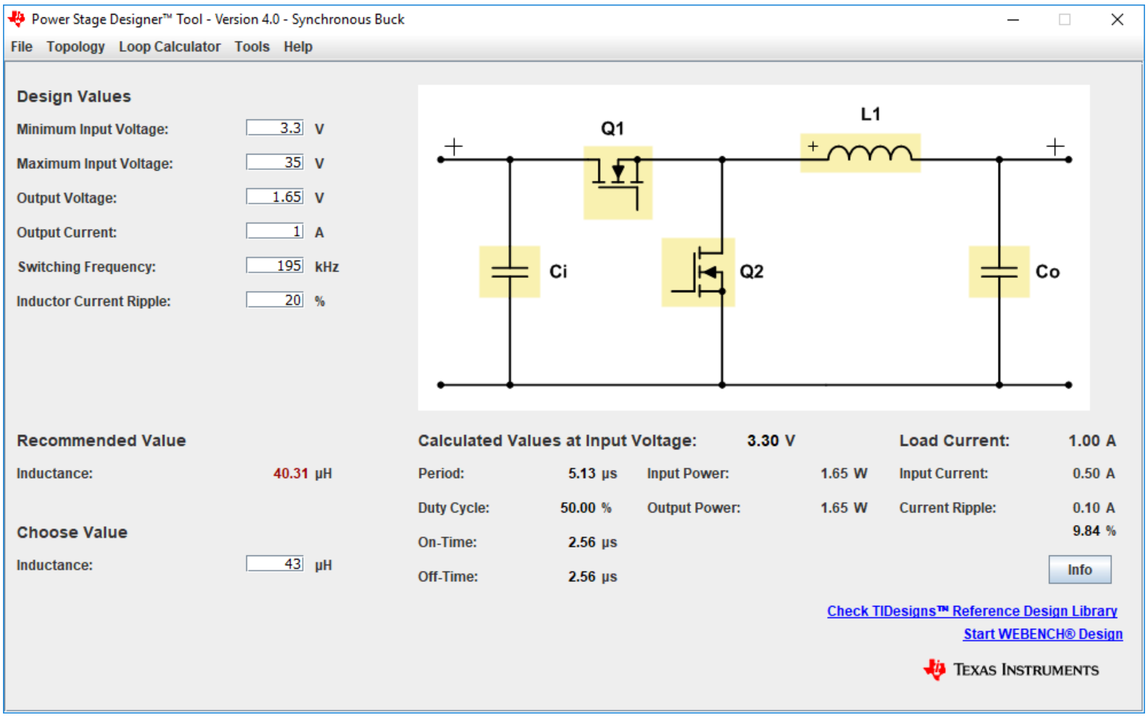


Figure 4.1: Power Stage Design Tool Simulation Result 1 [6]

According to Figure 4.1, the recommended inductor value is 40.31µH provided the output current is set at 1A. Thus, 43µH is selected.

Figure 4.2 below shows the result of selecting 33µH inductor by shorting the 10µH inductor. According to the result, the inductor current ripple is still within 20% that was set.

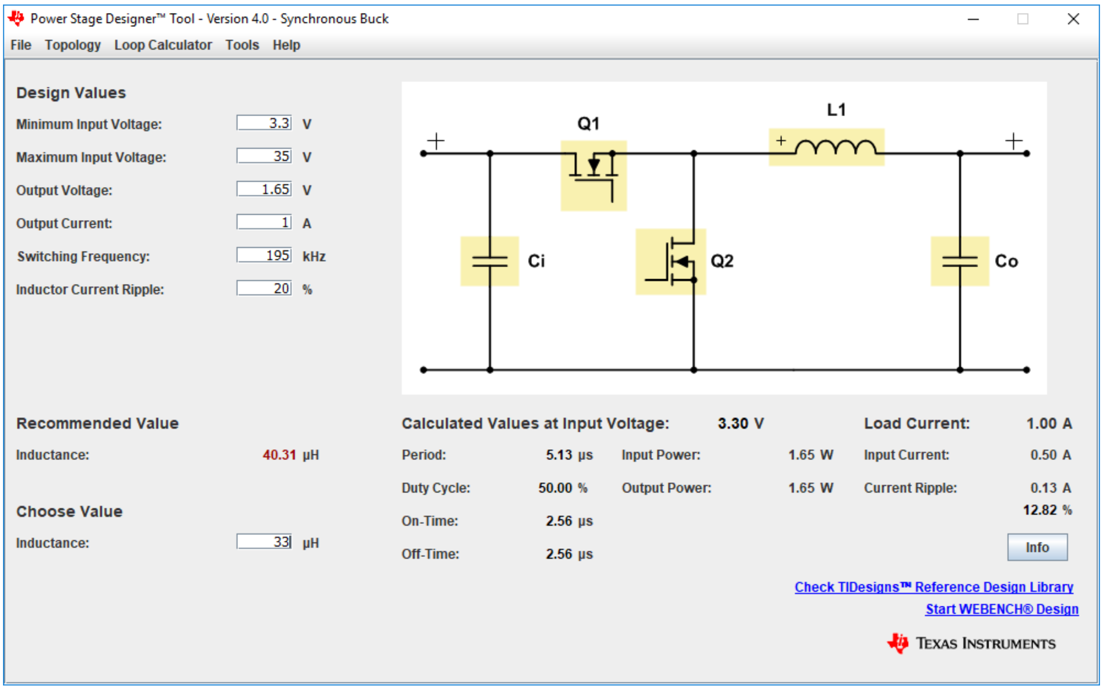


Figure 4.2: Power Stage Design Tool Simulation Result 2 [6]

4.2 External Gate Resistance

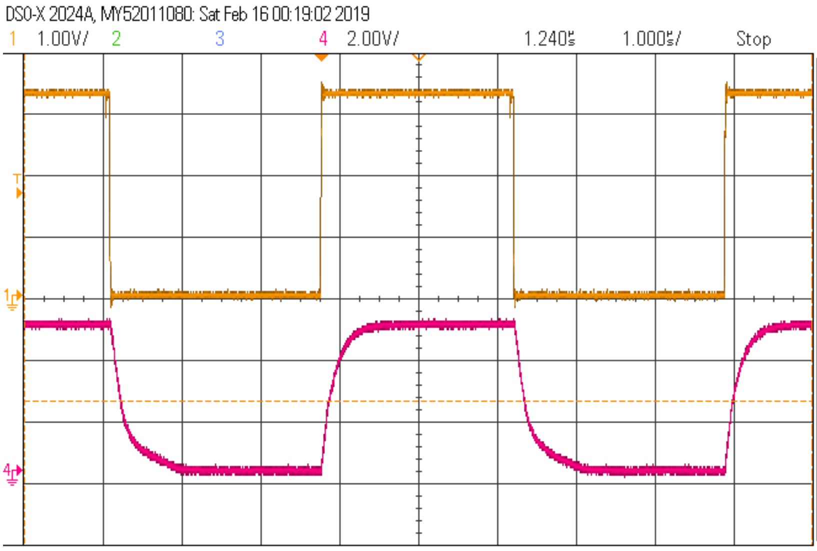
External gate resistor able to reduce the unwanted oscillation by damping the oscillation during switching and thus provide a smoother output. However, external gate resistor will result in switching delay. Therefore, a trade-off between fast rise and fall times versus oscillation results in the external gate resistor is a valuable element in the gate-drive design [2].

In this thesis, several gate resistors were tested and investigated in order to obtain the optimized external gate resistance for the trade-off between switching speed and oscillations.

4.2.1 High Gate Driver

Table 4.1, 4.2 and 4.3 show the overall waveform at the high side driver with the zoomed in rising and falling edge for comparison.

Table 4.1: Waveform for External Gate Resistance = 18Ω

External High Gate Resistance: **18Ω**		
Type of Waveform		**Output Waveform**
(a)	Overall with $R_G = 18\ \Omega$	

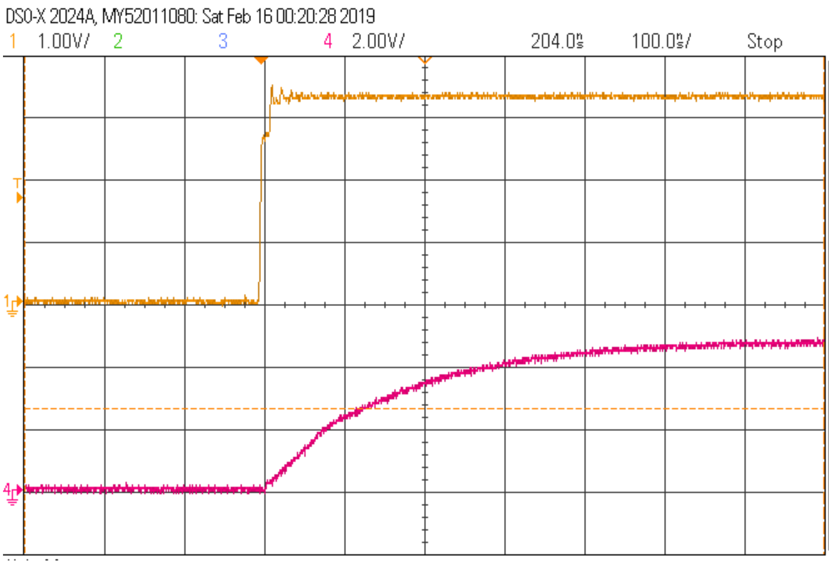
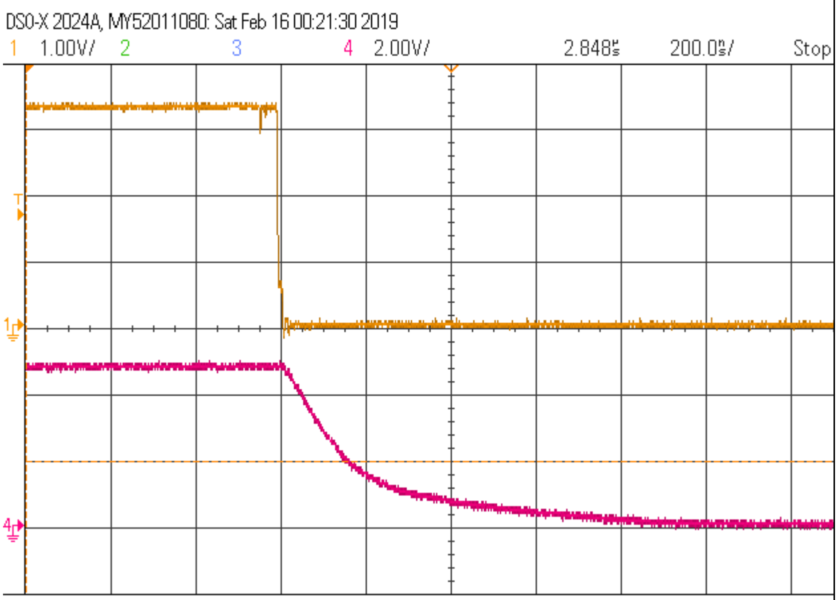
(b)	Rising Edge with $R_G = 18\ \Omega$	
(c)	Falling Edge with $R_G = 18\ \Omega$	

Table 4.2: Waveform for External Gate Resistance = 6.8Ω

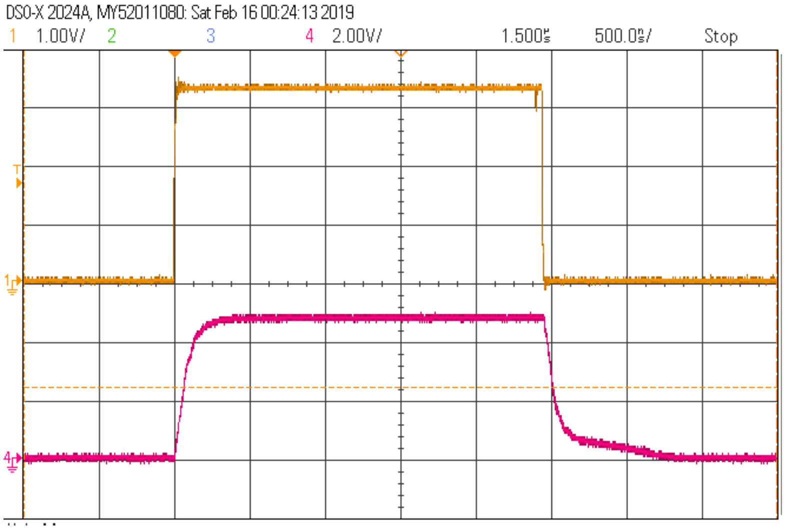
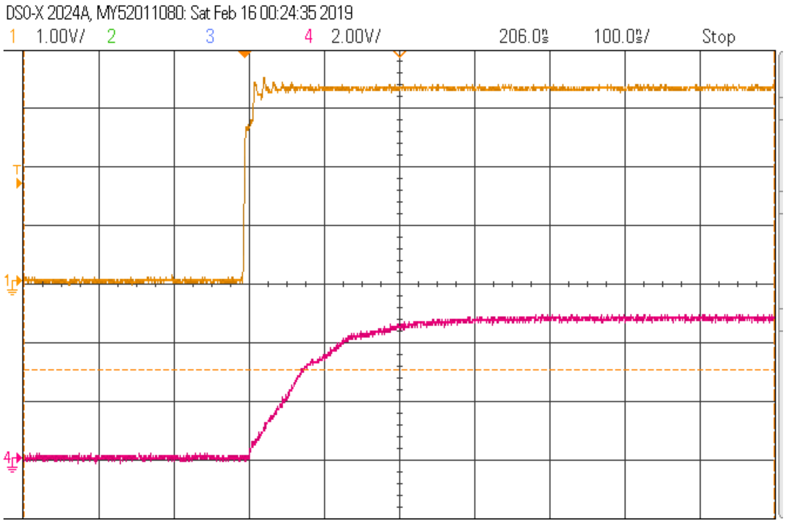
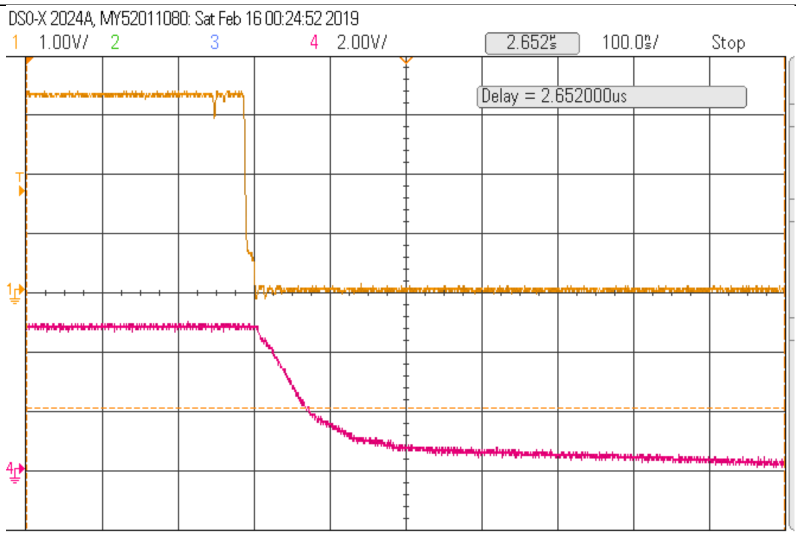
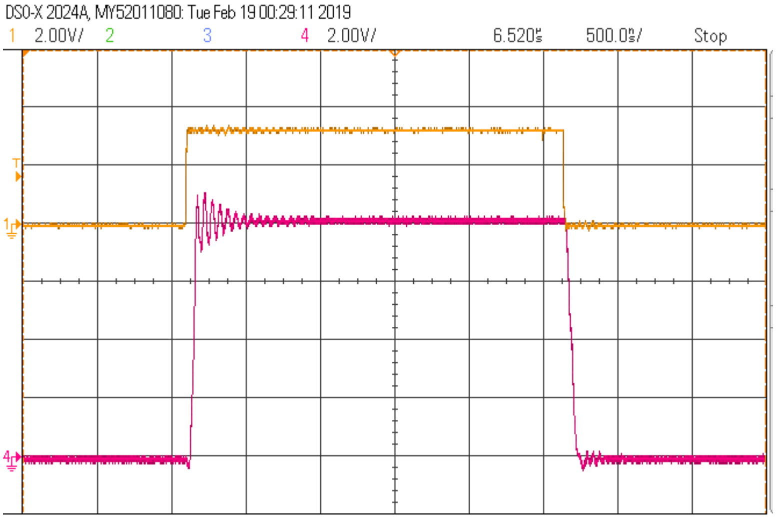
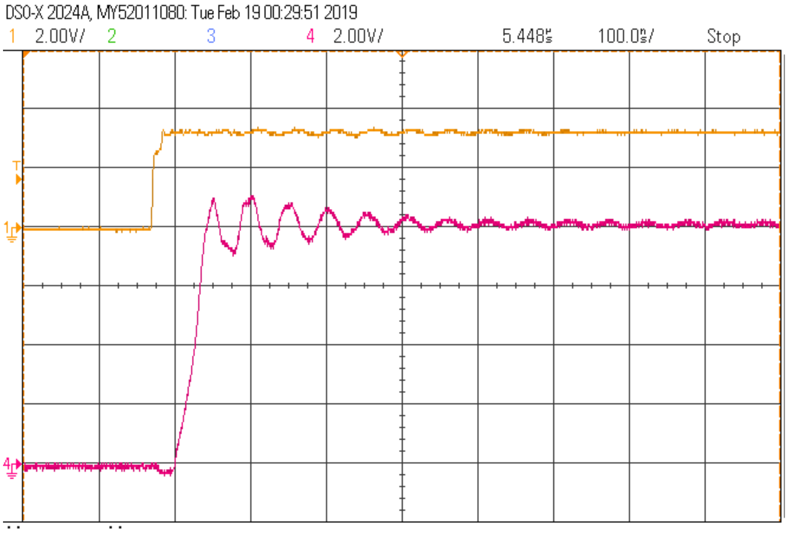
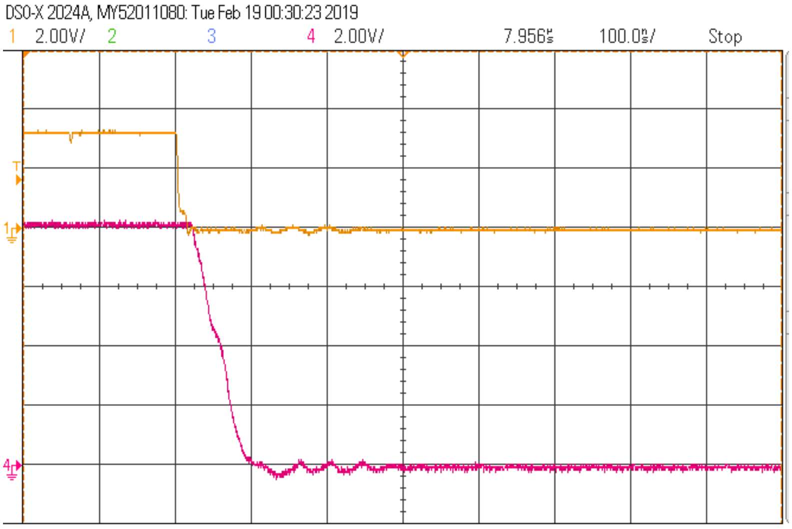
External High Gate Resistance: **6.8Ω**		
Type of Waveform		**Output Waveform**
(a)	Overall with $R_G = 6.8\ \Omega$	
(b)	Rising Edge with $R_G = 6.8\ \Omega$	
(c)	Falling Edge with $R_G = 6.8\ \Omega$	

Table 4.3: Waveform for External Gate Resistance = 0Ω (Short Circuit)

External High Gate Resistance: 0Ω (Short Circuit)		
Type of Waveform		**Output Waveform**
(a)	Overall with $R_G = 0\Omega$	
(b)	Rising Edge with $R_G = 0\ \Omega$	
(c)	Falling Edge with $R_G = 0\ \Omega$	

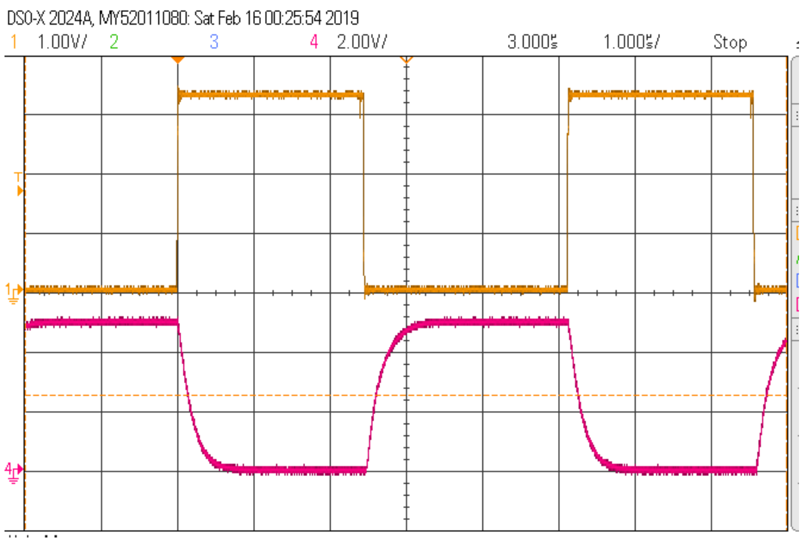
As investigated from the results above, the time required to achieve the gate threshold of the FET (2.5V) for 18 Ω, 6.8 Ω and no external gate resistance are approximately 150ns, 80ns and 20ns respectively. However, there is no significant overshoot in the switching when 18 Ω and 6.8 Ω external resistors are connected. An overshoot of nearly 1V can be seen when there is no external gate resistance connected.

In this design, fast switching time plays an important role as the high side FET must be fully switched off before the switching on of the low side FET to avoid a short circuit from V_{CC} to ground. Therefore, small oscillation or overshoot during the switching need to be accepted for trade-off.

4.2.2 Low Gate Driver

Table 4.4, 4.5 and 4.6 show the overall waveform at the low side driver with the zoomed in rising and falling edge for comparison.

Table 4.4: Waveform for External Gate Resistance = 20Ω

External High Gate Resistance: **20Ω**		
Type of Waveform		**Output Waveform**
(a)	Overall with $R_G = 20\ \Omega$	

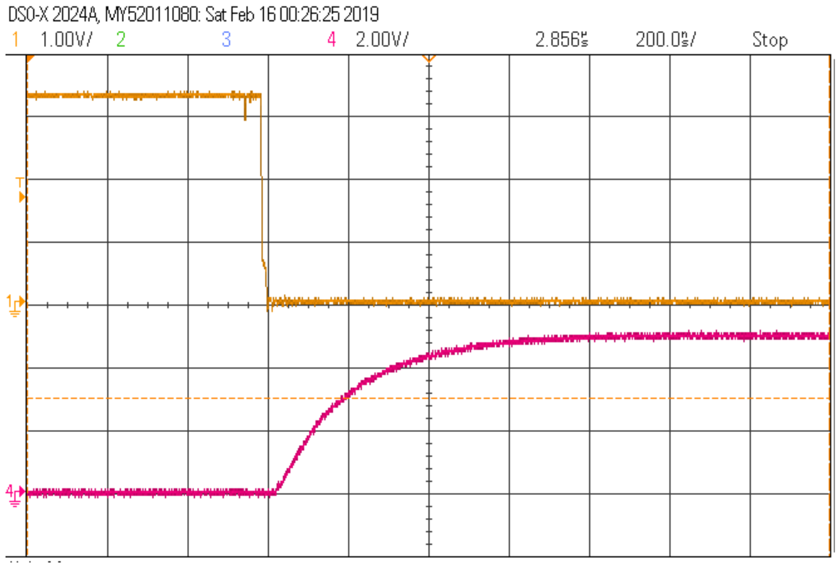
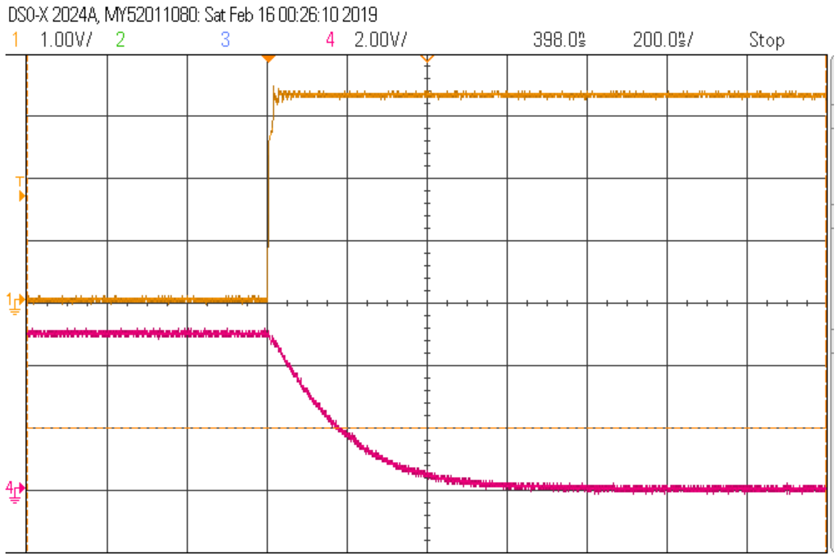
(b)	Rising Edge with $R_G = 20\ \Omega$	
(c)	Falling Edge with $R_G = 20\ \Omega$	

Table 4.5: Waveform for External Gate Resistance = 6.8Ω

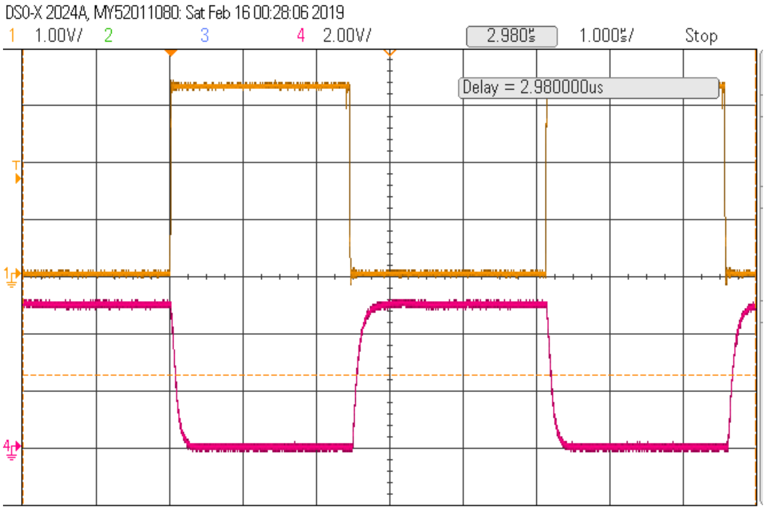
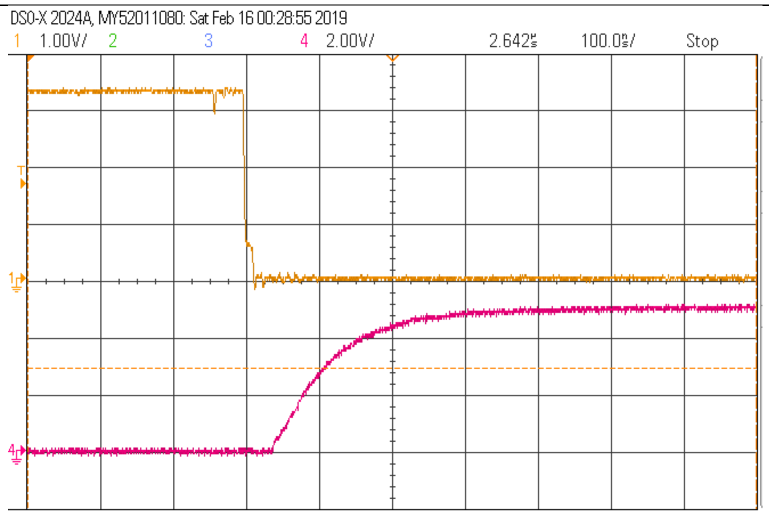
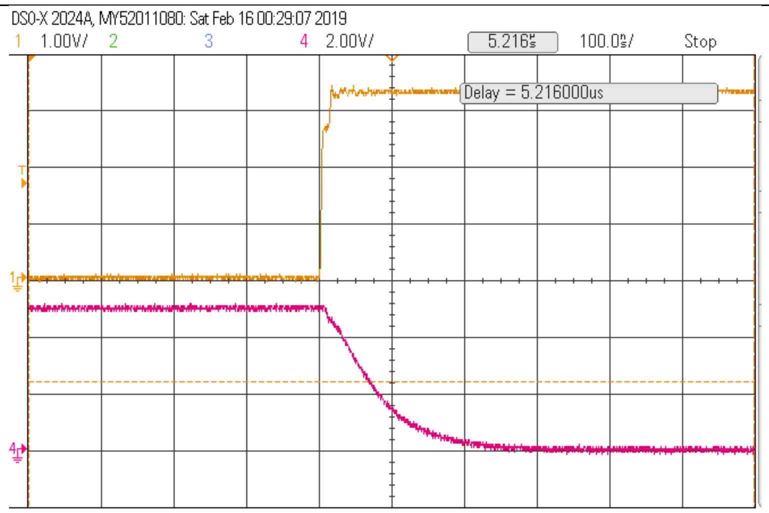
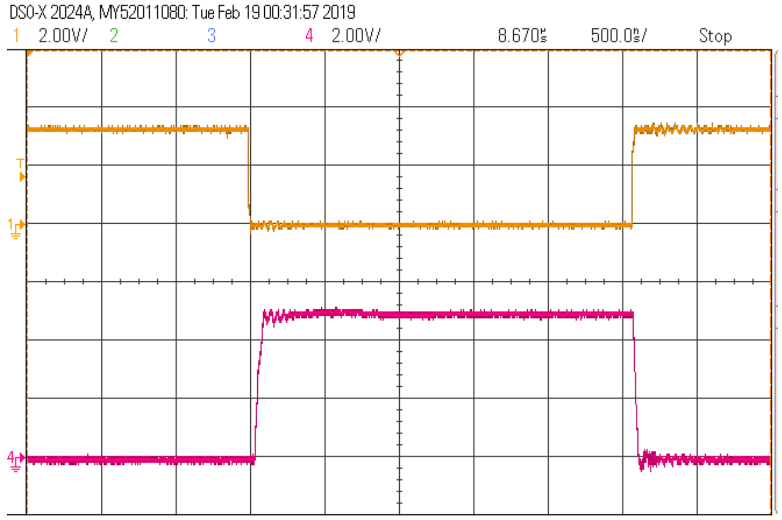
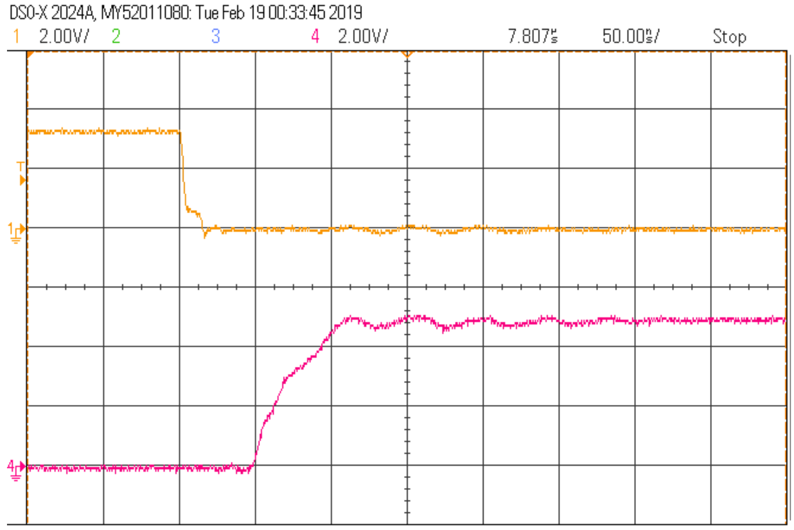
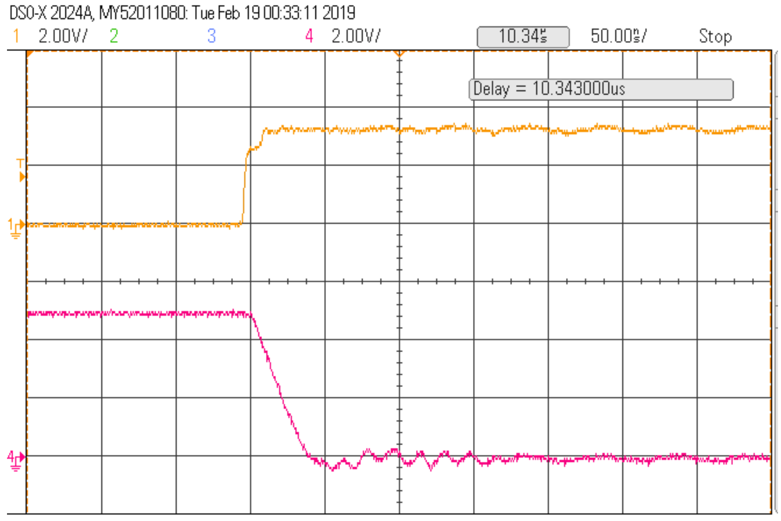
External High Gate Resistance: **6.8Ω**		
Type of Waveform		**Output Waveform**
(a)	Overall with $R_G = 6.8\ \Omega$	
(b)	Rising Edge with $R_G = 6.8\ \Omega$	
(c)	Falling Edge with $R_G = 6.8\ \Omega$	

Table 4.6: Waveform for External Gate Resistance = 0Ω (Short Circuit)

External Low Gate Resistance: **0Ω (Short Circuit)**		
Type of Waveform		**Output Waveform**
(a)	Overall with $R_G = 0\ \Omega$	
(b)	Rising Edge with $R_G = 0\ \Omega$	
(c)	Falling Edge with $R_G = 0\ \Omega$	

For the low side driver, it is similar with the high side driver where the switching time is critical for the design. Therefore, a minor oscillation was accepted during the selection of the external low side resistor. Considering the trade-off and measured heating of the Power FETs, no external resistor was connected for the design.

4.3 Summary

Both inductors and gate resistors play an important role in the design. The inductor was selected through the Power Designer software to ensure the output current ripple is within the range (typically 20%). In this design for a load current of 1A, 43 µH inductor is the most optimum inductance value.

On the other hand, switching speed and oscillation are the major issues to be investigated for the design of the buck converter. Different external gate resistors were tested for the design before coming to the conclusion of no external gate resistor was required for both high side and low side FETs.

CHAPTER 5

RESULTS AND DISCUSSIONS

5.1 DC/DC Buck Converter

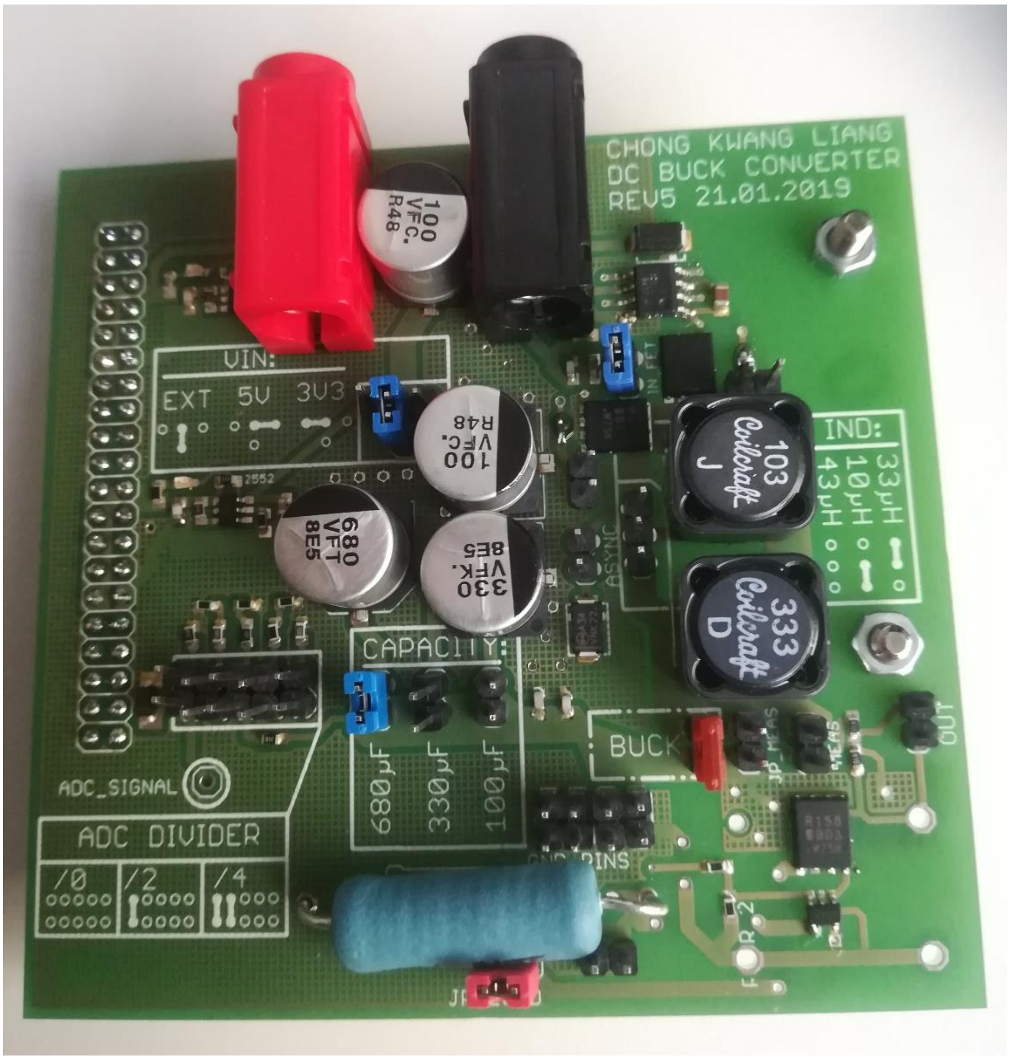


Figure 5.1: DC/DC Buck Converter PCB Board

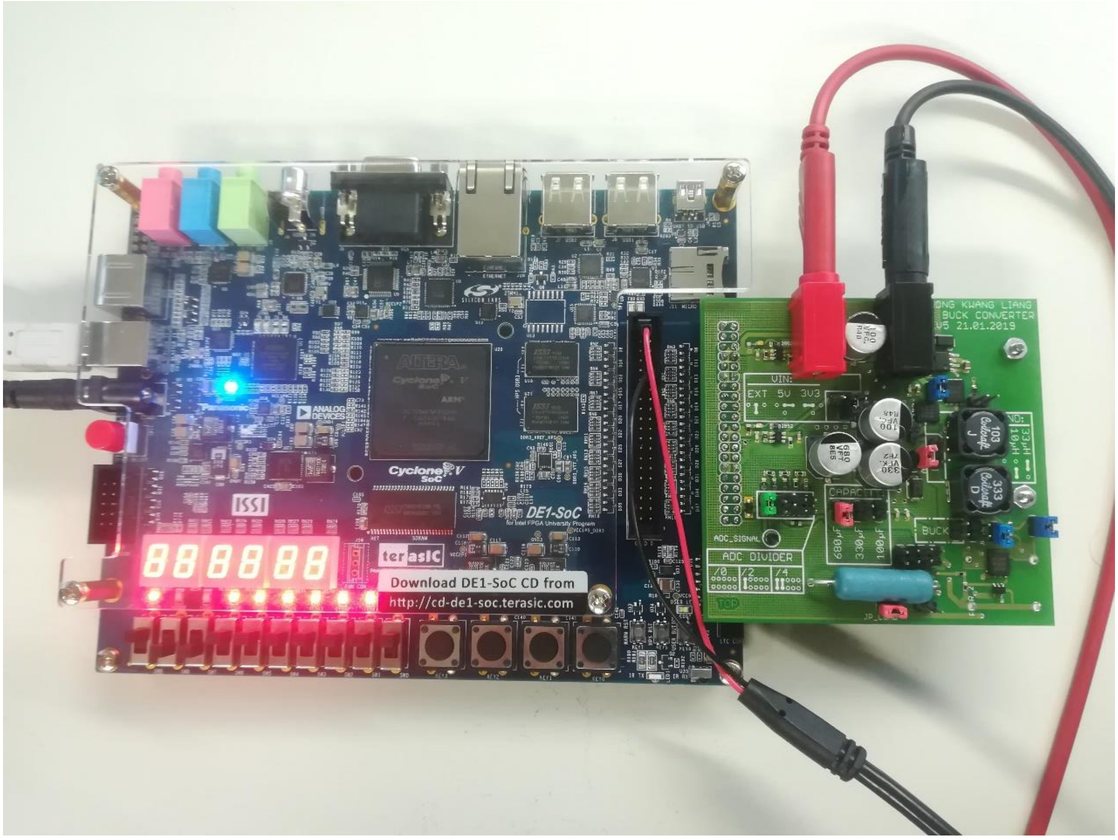


Figure 5.2: Buck Converter Board Interface with DE1-SoC FPGA Board

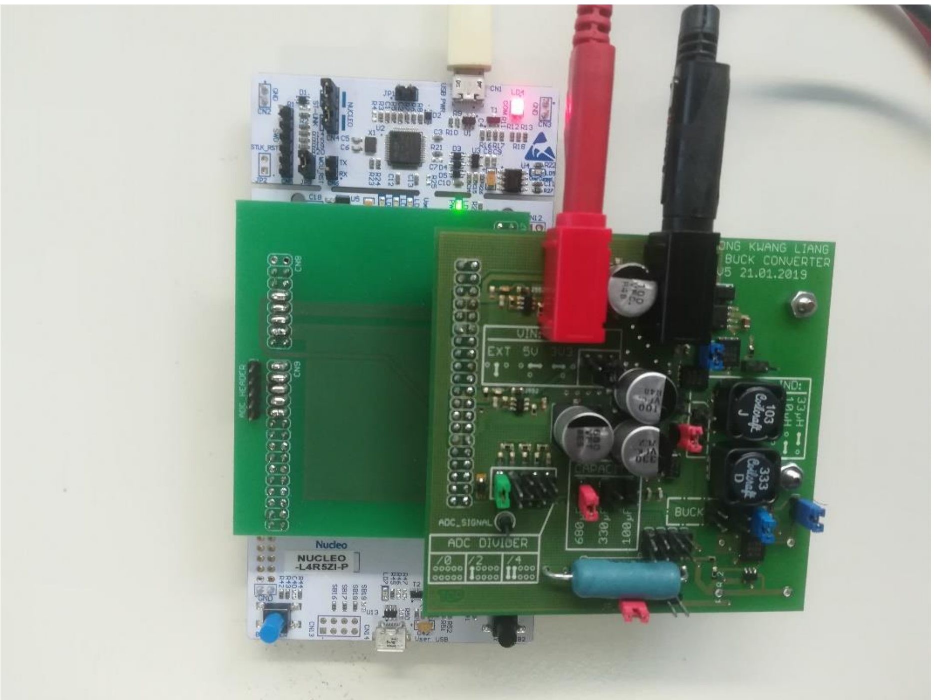


Figure 5.3: Buck Converter Board Interface with STM32 µC

5.2 Inductor Current

The inductor current is measured by measuring the voltage across 0.1Ω resistor that is connected in series with the inductor. The current is then computed by using Ohm's Law.

Figure 5.4 and Figure 5.5 show the output waveform of the voltage across the 0.1Ω resistor for loaded and unloaded condition respectively.

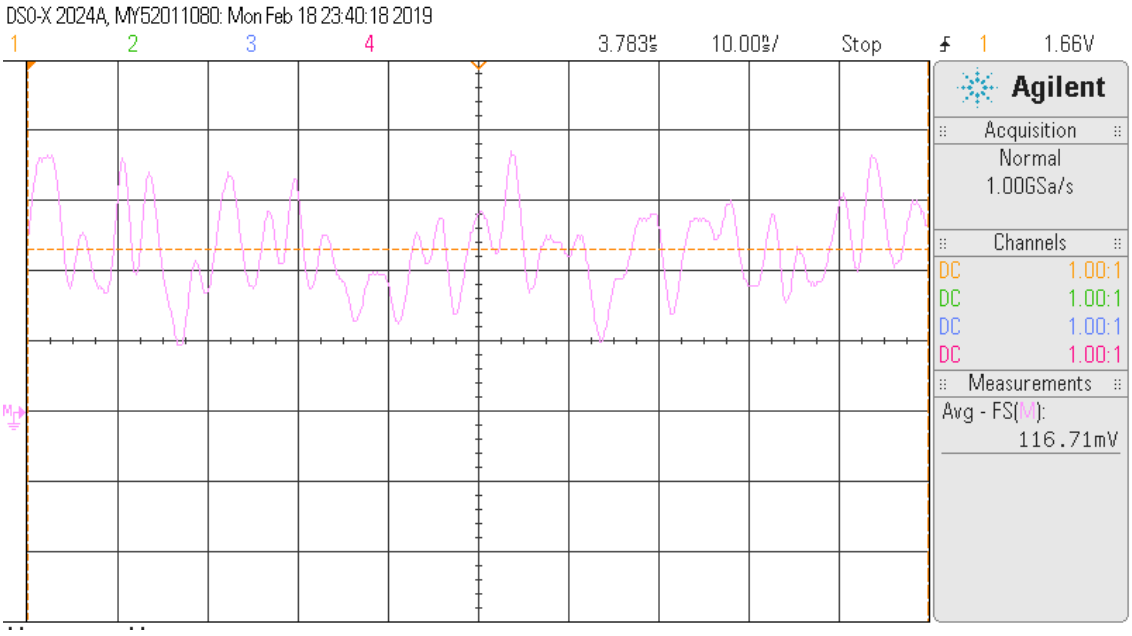


Figure 5.4: Waveform across 0.1Ω resistor when loaded

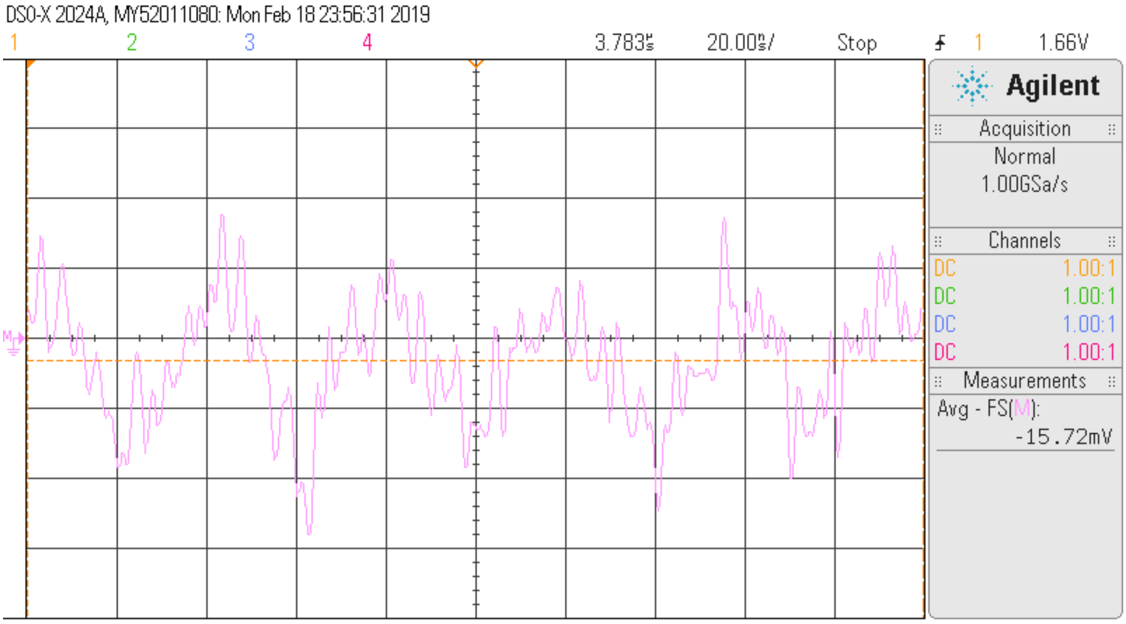


Figure 5.5: Waveform across 0.1Ω resistor when unloaded

During the loaded condition, the buck converter operates in continuous conduction mode (CCM) [4]. In this mode of operation, the inductor current will never fall below zero as shown in Figure 5.1 clearly.

During the no load or low load condition, there is negative current flowing through the inductor. The negative current is shunt to ground which results in the losing of power. This is known as discontinuous conduction mode (DCM) [4]. It is due to the low output current which will result in the inductor to reduce to less than zero eventually for a portion of switching time. Therefore, synchronous operation mode is not recommended for low current application.

5.3 Output Voltage

5.3.1 Unloaded Output

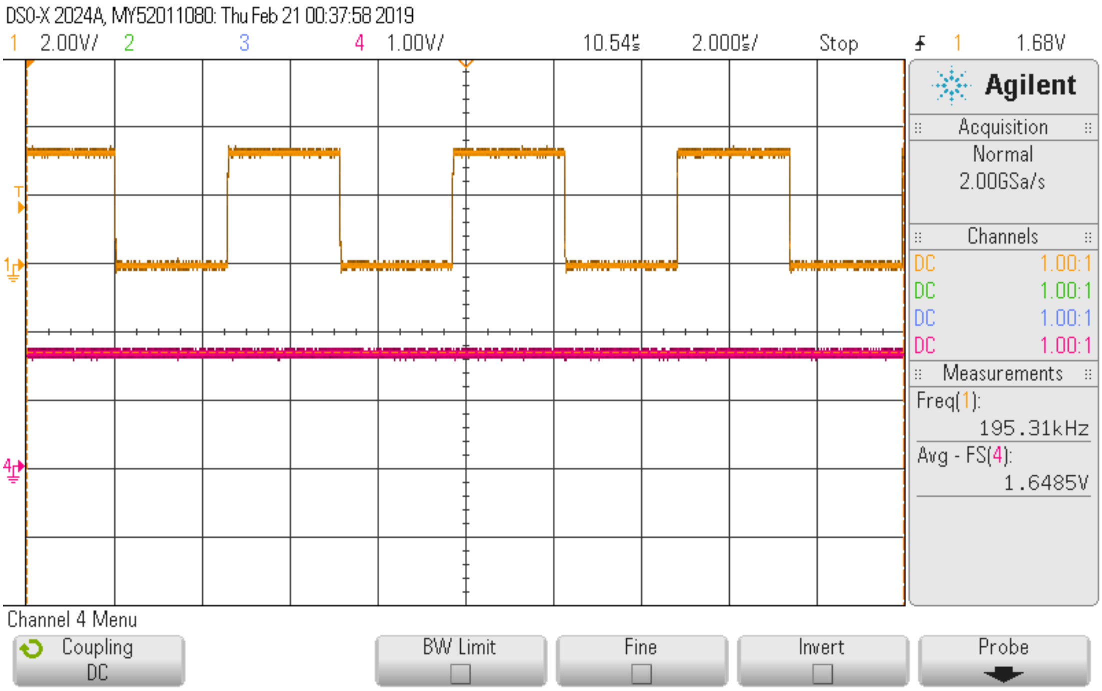


Figure 5.6: Output Waveform when Unloaded (DC Coupling)

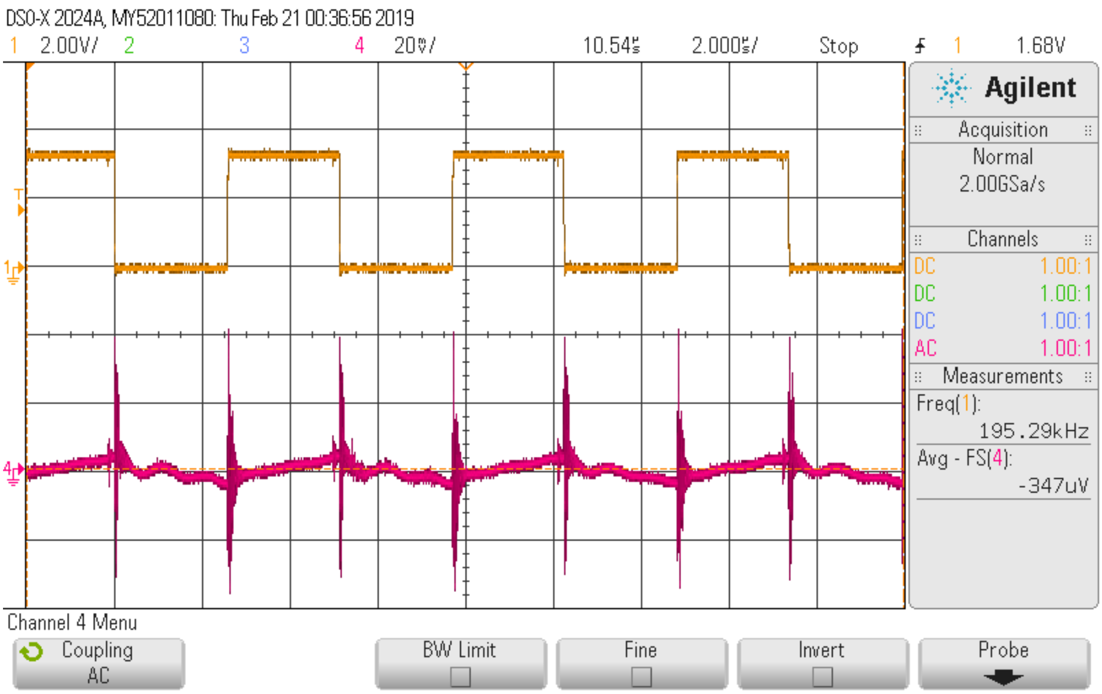


Figure 5.7: Output Waveform when Unloaded (AC Coupling)

Figure 5.6 and Figure 5.7 show the output voltages for both DC and AC coupling when the buck converter is operating in synchronous unloaded condition. As seen from the Figure 5.3, there is no significant oscillation when it is viewed with DC coupling. The peak to peak voltage is less than 80 mV for AC coupling. It is such a convincing and satisfying result obtained.

5.3.2 Loaded Output

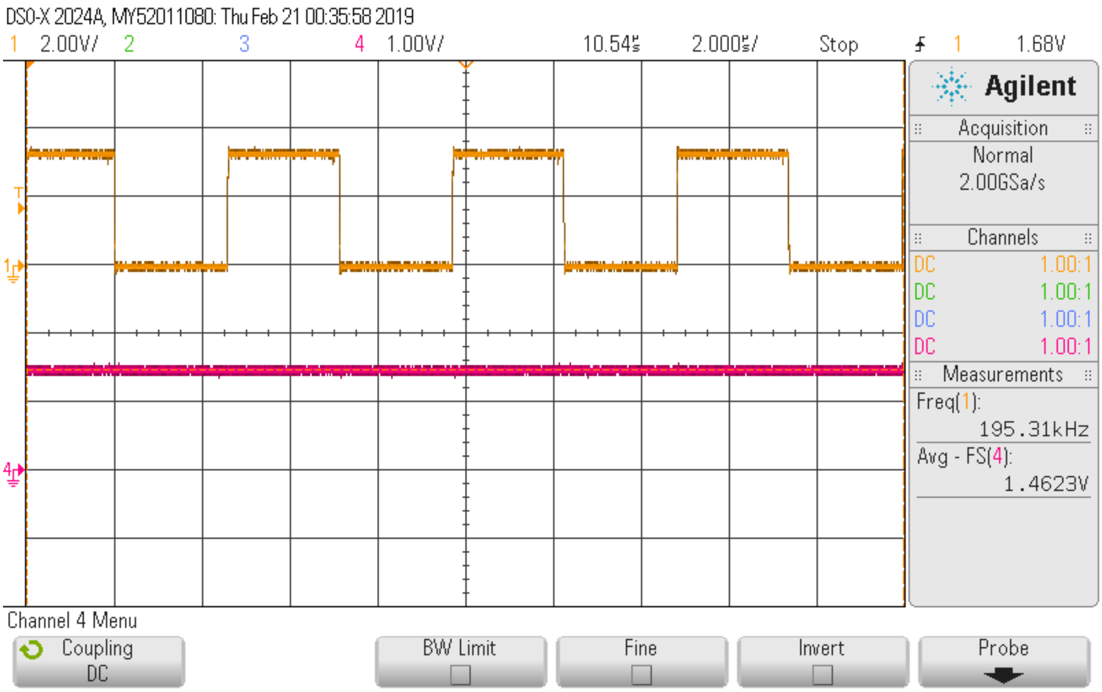


Figure 5.8: Output Waveform when Loaded (DC Coupling)

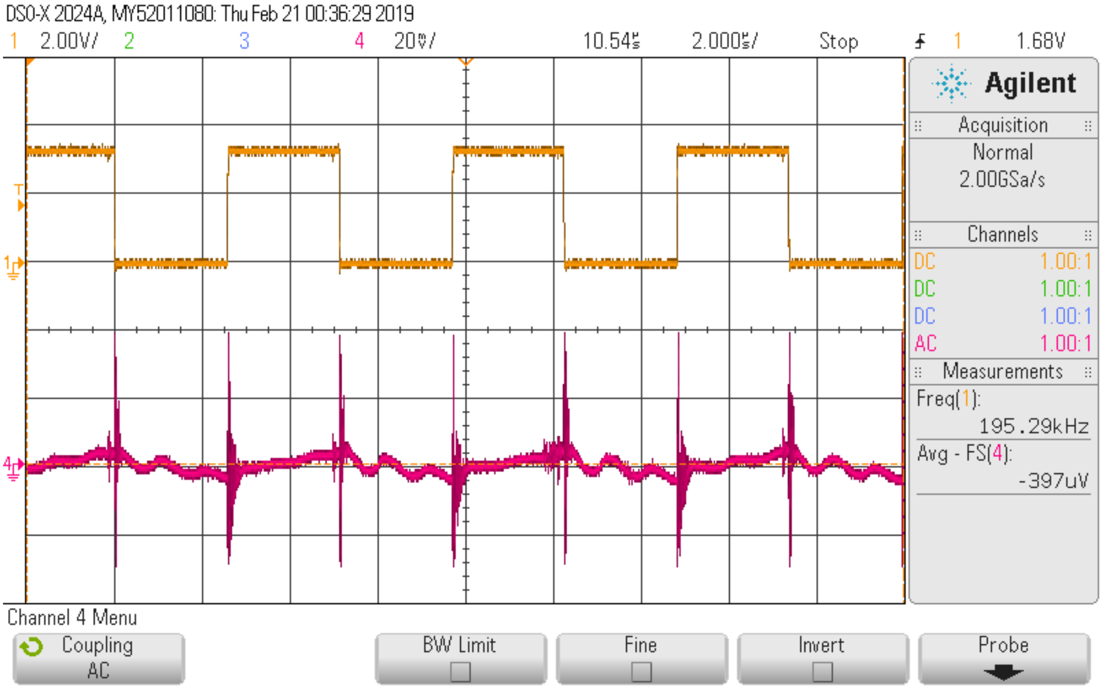


Figure 5.9: Output Waveform when Loaded (AC Coupling)

As there is no control loop in this testing, the slight drop of voltage is expected. The effective R_{out} can be computed as follow:

When I_L = 0A, V_{out} = 1.649V

When I_L = 1A, V_{out} = 1.462V

$$R_{out} = \frac{V_{out}}{I_L}$$

$$= \frac{(1.649-1.462)V}{(1-0)A}$$

$$= \mathbf{187\ m\Omega}$$

There is no significant oscillation even with loaded circuit during the DC coupling and the oscillation in AC coupling remains. Thus, it is quite convincing result.

CHAPTER 6

CONCLUSION AND RECOMMENDATIONS

6.1 Conclusion

A DC/DC Buck Converter had been designed and certain parameters have been investigated such as the inductance value and the external gate resistance. The output waveform is optimized with minimum oscillation. The board is ready to be plugged in both FPGA (DE1-SoC Board) and microcontroller (STM32L4R5 board aided by interface board). Therefore, digital control of the buck converter can be concluded and investigated in near future.

6.2 Recommendations for Future Work

The control of the DC/DC buck converter digitally by using FPGA and microcontroller will be an interesting field to study. The comparison of FPGA and microcontroller performance in the digital control is the main interest. With the working DC/DC buck converter board, detailed research on the digital control can be done in near future.

Moreover, design of boost converter will be an interesting topic to study as well. Buck converter normally did not work independently. It will be interesting if there is a working boost working where control of buck-boost converter can be carried out.

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