RED: Rechnergestützter Entwurf Dig+A1:M20ital // Rule-Based Electronic Design 27.03.2020

	class	Rechnergestützter Entwurd Digital			days	Date	Lab	Practical Training of RED
					diff.	Thursday		
#	Room	**Contents RED**	**proj.**	**scored**		**new**	Room	**Practical Training**
1	S043	1 Introduction	1,04		7	23.04.2020	home	Install + test Intel tools: ModelSim, Quartus
2	S043	2.1 FSM	2,09		7	30.04.2020	home	Appendix: (i) Get Start w. ModelSim+QuartusII
3	S043	2.2 Rules for Digital Circuit Design	2,14		7	07.05.2020	home	(ii) ModelFile4Studs\VHDL\lib_flat > wstart.mpf
4	S043	2.2 Rules for Digital Circuit Design: Exercises	2,18		7	14.05.2020	home	
5		no lectures	2,18		7	21.05.2020	home	Program and run examples with ModelSim of what you learn
6	S043	3. VHDL Design Units:, Entity, Archit, Config.	3,11		7	28.05.2020	home	in Section "3. VHDL Based Design"
7	S043	3. VHDL Code Types: Conc., Struct, Sequ	3,20		7	04.06.2020	home	
8		no lectures	3,20		7	11.06.2020	home	
9	S043	3. VHDL Data: Libs, ModelSim: create package	3,25		7	18.06.2020	home	Install + test Matlab / Simulink
10	S043	3. VHDL: Design for Synth., FSM: 1+2 process	3,29		7	25.06.2020	home	Program and run examples with Matlab of what you learn
11	S043	3. VHDL: Directory Structure, LTI, IIR-Filt,	3,37		7	02.07.2020	home	in Section 4 + 5 LTI and Cycle-Based Desgin with Matlab
12	S043	3. VHDL: IIR filter design, -> do with ModelSim	3,42		7	09.07.2020	home	
13	S043	4. Matlab cycle-based FSM modleling 1	4,10		7	16.07.2020	home	
14	S043	5. LTI systems with Matlab: run & read models	5,10		7	23.07.2020	home	5. LTI systems with Matlab: run & read models
15	S043	6. Ltspice + Simulink: run & read models	6,10		7	30.07.2020	home	6. Ltspice + Simulink: run & read models
16		Semester ends			7	06.08.2020	home	Semester ends