4 VHDL-AMS Fundamentals

AMS: Analog and Mixed Signal Extensions to VHDL

Definition: "VHDL-AMS is a strict superset of VHDL 1076-1993:

\[
\text{VHDL-AMS} = \text{IEEE VHDL 1076-1993} + \text{IEEE VHDL 1076.1-1998}
\]

4.1 Introduction to VHDL-AMS

Complex systems often require both analog and digital simulation. In addition, shrinking device dimensions and ever increasing frequencies created a need for a Microwave HDL (MHDL) and an Analog HDL (AHDL or HDL-A). On this background VHDL-AMS (AMS = Analog and Mixed Signals), formally termed "VHDL 1076.1", was developed.

A major goal during the development of VHDL-AMS was to maintain the fundamental ideas of top-down design and behavioral modeling.

VHDL-AMS is a superset of VHDL. In other words: VHDL-AMS supports VHDL plus specific statements made for analog and mixed signal modeling.

The two new data objects QUANTITY and TERMINAL are added to the known three data objects SIGNAL, VARIABLE, CONSTANT. Furthermore a NATURE being something like a specific data type is introduced.

A QUANTITY is a real value with an analog time axis represented by real numbers. VHDL-AMS has to handle two time axis: the digital time axis represented as an integral multiple of the time base (i.e. fs), and the analog time axis represented by real numbers. The management of those two time axis is an internal problem of VHDL-AMS. A QUANTITY is initialized with 0.0 by default.

A TERMINAL consists of two QUANTITYs, one ACROSS quantity (e.g. voltage) and one THROUGH quantity (e.g. current).

The NATURE of a TERMINAL is something like a data type. The NATUREs electrical, thermal, fluid_mechanics may have ACROSS quantities of voltage, temperature, pressure and THROUGH quantities of current, heat_flow, flow_rate, respectively.

This chapter intends to make the reader aware of VHDL-AMS and to give him a first idea of how it works. For more detailed information the reader is referred to the respective literature, e.g. [4.1], [4.2], [4.3].

Exercise 4.1-1:

a) What does "AMS" in the term VHDL-AMS stand for?

b) What is the formally correct name for this standard?

c) What restrictions must be made to digital VHDL to be compatible with VHDL-AMS?
4.2 Analog Circuit Description

Figure 4.1:

Fig. 4.1 shows a typical problem arising for high speed digital circuits: Get high speed signals from an external pin to the internal semiconductor chip. The bond wire is an inductor, the overvoltage protection system is a diffusion resistor followed by protection diodes with large junction capacitances. A possible source code to model the system of Fig. 4.1 using VHDL-AMS is shown below.

(1) PACKAGE pk_electrical;
(2)   SUBTYPE voltage IS REAL;
(3)   SUBTYPE current IS REAL;
(4)   NATURE electrical IS voltage ACROSS current THROUGH;
(5) END PACKAGE pk_electrical;
(6)
(7) USE WORK.pk_electrical.ALL;
(8) ENTITY filter IS
(9)   PORT(TERMINAL Npin,Nchip: electrical)
(10) END filter;
(11)
(12) ARCHITECTURE arc_filter OF filter IS
(13)   CONSTANT inductor: REAL:=6.0E-9;    -- 6 nH
(14)   CONSTANT resistor: REAL:=60.0;      -- 60 Ohms
(15)   CONSTANT capacitor: REAL:=12.0E-12; -- 12 pF
(16)   TERMINAL Nx: electrical;
(17)   QUANTITY vl ACROSS il THROUGH Npin TO Nx;
(18)   QUANTITY vr ACROSS ir THROUGH Nx TO Nchip;
(19)   QUANTITY vc ACROSS ic THROUGH Nchip; -- TO ground
(20) BEGIN
(21)   vr == resistor * ir;
(22)   vl == inductor * il'DOT;
(23)   ic'INTEG / capacitor == vc;
(24) END arc_filter;

Listing 4.1: VHDL-AMS source code example of the analog RLC input pad system

Lines 13, 14, 15 of the source code above declare three real type CONSTANTs containing the inductivity of the inductor, the resistance of the resistor and the capacitance of the capacitor, respectively. CONSTANTs are known from VHDL.
The ENTITY PORT declaration of line 9 declares Npin, Nx, Nchip to be TERMINALS of the NATURE electrical. (A PORT may contain both digital SIGNALs and analog TERMINALS.)

The QUANTITY declaration in line 17 declares the quantity vl to be an ACROSS quantity from TERMINAL Npin to TERMINAL Nx and il to be a THROUGH quantity from TERMINAL Npin to TERMINAL Nx.

The QUANTITY declaration in line 18 is very similar to that in line 17.

The QUANTITY declaration in line 19 declares vc to be an ACROSS quantity from TERMINAL Nchip to ground and ic to be a THROUGH quantity from TERMINAL Nchip to ground. As the second TERMINAL is omitted in this declaration, ground it taken by default.

Line 22 describes the behavior of the resistor: "vr==resistor*ir;". The operator "==" indicates simultaneous modeling: The right and the left hand side expressions of the equation are treated to be identical over the whole time axis. The general form of the simultaneous statement is

\[ g == h; \]

with g and h being analog expressions. The systems solves \( f=0 \) with \( f=g-h \).

Line 21 models the inductor using the attribute 'DOT to indicate the derivative with respect to time: The expression \( q' \cdot \text{DOT} \) corresponds to \( dq/dt \).

There is also an attribute 'INTEG available, indicating the integration with respect to time. However, integration comes along with integration constants and usually derivatives are employed if possible.

Line 23 models the capacitor using the expression \( vc' \cdot \text{DOT} \) to model \( dv_c/dt \).

A limited range of problems of other disciplines such like thermo dynamics, mechanics or fluid mechanics can be modeled with VHDL-AMS. The precondition is that the problem can be modeled using compact, discrete components.

Exercise 4.2-1:

a) Compute the pole frequencies of the RLC filter in Fig. 4.1 with the values taken from Listing 4.1 \( \omega_{p12} = R/2L \pm \sqrt{(R/2L)^2 - 1/LC} \).

b) What is the formally correct name for the VHDL-AMS standard?

c) Complete the following graphics by writing voltage names to the bent arrows and current names to the straight arrows in compliance with the declarations made in Listing 4.1.
d) What is the basic difference between Spice like simulators and the analog part of VHDL-AMS regarding system description?

e) Write a simultaneous statement using current $i$ and voltage $u$ to describe the behavior (i) of a capacitor $cap$ and (ii) to describe the behavior of an inductor $ind$.

f) What additional data objects are introduced in VHDL-AMS compared to VHDL?

g) When several TERMINALs are connected together, which law of Kirchhoff does then hold for the THROUGH quantities?

h) When several TERMINALs are connected together, which law does then hold for the ACROSS quantities?

i) Consider the following QUANTITYs belonging to the NATUREs electrical, thermal, fluid_dynamics: pressure, waterflow, voltage, heatflow, current, temperature. Write three QUANTITY declaration statements that declare those quantities from point $p_1$ to $p_2$ and distinguish between ACROSS and THROUGH quantities.

j) Can any mechanical problem be modeled with VHDL-AMS?
4.3 AMS Statements

4.3.1 IF USE

For D/A conversion VHDL-AMS adds the concurrent IF-statement

\[
\text{IF condition USE ... }
[\text{ELSIF condition USE ...}]
[\text{ELSE USE ...}]
\text{END USE;}
\]

**Figure 4.3.1:**
The logic signal `switch` has impact on the quantities `U_switch` and `I_Switch`.

```
LIBRARY ieee;
USE ieee.electrical_systems.ALL;
ENTITY switch IS
  GENERIC(R_switch:REAL:=0.01);
  PORT (SIGNAL switch_on:IN BIT;
       TERMINAL N1, N2:ELECTRICAL);
END switch;

ARCHITECTURE arc_switch OF switch IS
  QUANTITY U_switch ACROSS I_switch THROUGH N1 TO N2;
BEGIN
  IF switch_on='1' USE
    U_switch == R_switch * I_switch;
  ELSE
    I_switch == 0.0;
  END USE;
  BREAK ON switch_on;
END arc_switch;
```

**Listing 4.3.1:** VHDL-AMS Schaltermodell zum Stromlaufplan

Note that Listing 4.3.1 is a form of D/A conversion.
4.3.2 BREAK

BREAK initial_condition_1, ..., initial_condition_n;
BREAK ON object_1, object_2, ..., object_n;

The BREAK statement lists initial conditions or objects that can trigger discontinuities in the analog part of the solver, that require re-initialization. In the switch-model above an event on signal switch_on will cause a discontinuity of Rswitch and Iswitch. (Theoretically the simulator could work without BREAK statements. However, finding all possible discontinuities without the help of BREAK is like finding a needle in a haystack.)

4.3.3 Q'ABOVE statement:

- Q'ABOVE(E) is a Boolean signal,
  - FALSE when the value of Quantity Q is below the threshold E,
  - TRUE when the value of Quantity Q is above the threshold E,
- Q must be a scalar quantity,
- E must be an expression of the same type as Q,
- An event occurs on signal Q'ABOVE(E) at the instant of the threshold crossing,
- A process can be sensitive to that event.

4.3.4 S'RAMP

S'Ramp(rise_time, fall_time)

- Follows signal S with specified rise and fall times. Specify time with real values.

LIBRARY ieee;
USE ieee.electrical_systems.ALL;
ENTITY test_ramp_slew IS
END test_ramp_slew;
ARCHITECTURE arc_test_ramp_slew OF test_ramp_slew IS
  SIGNAL clock:BIT;
  SIGNAL clock_voltage:REAL:=0.0;
  QUANTITY U_ramp, U_slew:VOLTAGE; -- free Quantities
BEGIN
  clock <= NOT clock AFTER 5 ns;
  clock_voltage <= 4.0 WHEN clock='1' ELSE 0.0;
  U_ramp == clock_voltage'RAMP(1.0E-9,2.0E-9);
  U_slew == clock_voltage'SLEW(2.0E9,-1.25E9);
END arc_test_ramp_slew;

Listing 4.3.4: VHDL-AMS Code illustrating the attributes S'RAMP und S'SLEW, Q'SLEW.
4.3.4 \textbf{QUANTITIES} \texttt{U\_ramp} and \texttt{U\_slew} following signal \texttt{clock\_voltage} with given ramp widths and maximum slopes.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure4.3.4.png}
\caption{Example graph showing \texttt{clock\_voltage} and \texttt{U\_ramp}, \texttt{U\_slew} over time.}
\end{figure}

\subsection*{4.3.5 S'\textsc{SLEW} and Q'\textsc{SLEW}}

\texttt{S'\textsc{Slew}}(\texttt{max\_rising\_slope}, \texttt{max\_falling\_slope})

\texttt{Q'\textsc{Slew}}(\texttt{max\_rising\_slope}, \texttt{max\_falling\_slope})

- follows Signal S or Quantity Q, respectively, but derivatives are limited to the specified slopes.
- Experience of the author: S'\textsc{SLEW} works well, Q'\textsc{SLEW} often problematic.

\section*{4.4 References}

