2 Quantization

2.1 Introduction to A/D and D/A Conversion

2.1.1 Interfaces Between the Analog and Digital World

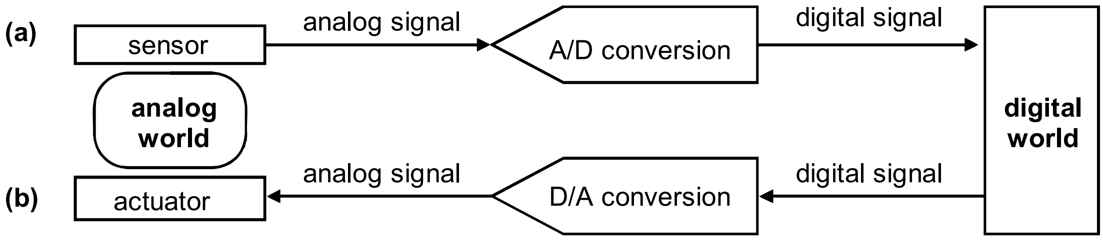


Fig. 2.1.1: Example for: **(a)** A/D conversion, **(b)** D/A conversion

A signal is the physical representation of an information. It is independent of the particular medium that transports it, which can be water, gas, a voltage or current or electromagnetic wave, etc. A long time ago people carved characters in stone, and this technique has survived in cemeteries to this day. The Romans transmitted signals with flags and this is still the case today at airports. This communication is focused on voltages.

Fig. 2.1.1 illustrates A/D and D/A conversion, where A/D conversion is significantly more complex: It comes with both quantization error and time-discretization.

A/D conversion is a two-dimensional process: discretization in value und time domain

Table 2.1.1 list the converters presented in this documentation. Subsection 2.2 presents three D/A converter architectures (equally and binary weighted summation, R-string) and subsection 2.3 presents three A/D converters architectures (SAR, flash and semi-flash, pipelined) that sample at Nyquist rate. Furthermore, both subchapters show how the three oversampling types (PWM, Δ and ΔΣ modulator) can be operated in both directions, namely digital-to-analog and analog to-digital. Section 2.4 resolves some acronyms and presents quality criteria.

Table 2.1.1: Data converter types presented in this chapter

Type	D/A converters	A/D converters
Nyquist sampler	equally weighted	SAR
	binary weighted	Flash and Semi-Flash
	R-string	Pipelined
over sampler	PWM: Pulse-Width Modulation	PWM: Pulse-Width Modulation
	Δ Modulation & Demodulation	Δ Modulation & Demodulation
	ΔΣ Modulation & Demodulation	ΔΣ Modulation & Demodulation

2.1.2 Accuracy Considerations

Accuracy considerations

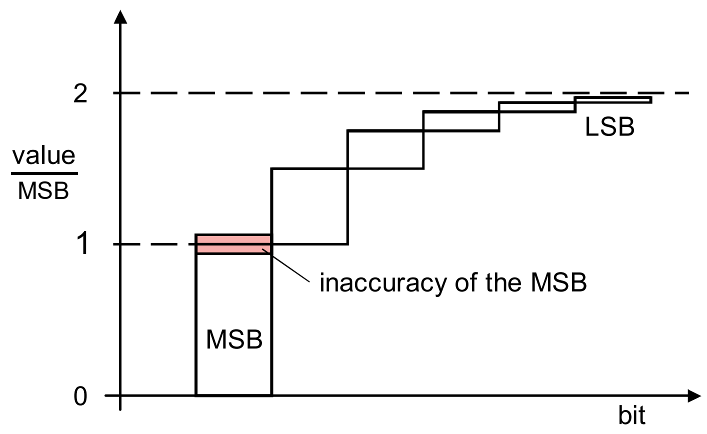
Relative accuracy specifications are typically given in percentage of the maximum. With *NoB* standing for *Number of Bits* or *bit-width*, the range of integral numbers is 0 … $2^{NoB} - 1$ for unsigned and -2^{NoB-1} … $2^{NoB-1} - 1$ for signed integer.

"Accuracy of 1%" does typically not mean 1% of the actually measured value, but 1% of the possible maximum value. An error of 1% of 2V is 20mV, independently of the actually measured value.

The Meaningful Number of Bits

Fig. 2.1.2 illustrates that for instrumentation purposes the error of the MSB must be less than or equal to half of the required minimum step, frequently termed Δ, because it is pointless to evaluate bits whose impact is less than the error of the MSB.
However, if we hear sound, then we perceive noise relative to the actual amplitude. A typical music CD supports 16 bits per sample, while we typically hear a signal-to-noise ratio (*SNR*) of some 10...12 bits.

Fig. 2.1.2:
Least significant bits make no sense if their impact is less than the error caused by the most significant bits.



2.1.3 Limit-Cycling

2.2 Digital-to-Analog Converters (DACs)

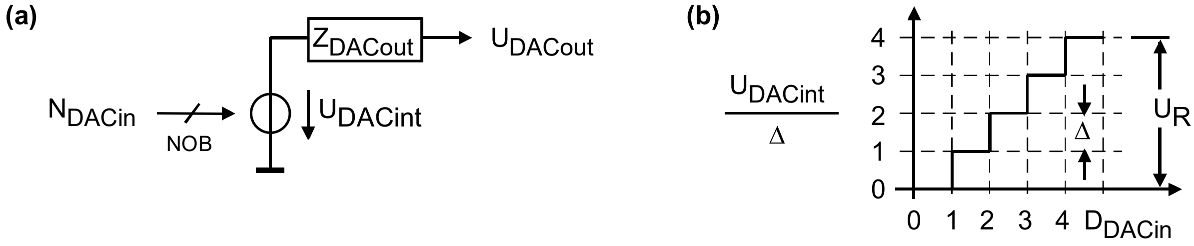


Fig. 2.2: (a) Equivalent D/A converter model, **(b)** *NoL* levels comprise (*NoL-1*) Δ's

Fig. 2.2(a) illustrates the principle of a digital-to-analog converter (DAC) with electrical voltage output. A *NoB* bit wide digital input word causes an inner source voltage U_{src}. Depending on the electric load and output impedance Z_{DACout} we measure the output voltage U_{DACout}. Some DACs may output other analog quantities such as current or impedance, but most DACs deliver voltages. A delta (Δ_{DA}) represents a minim step corresponding to a change of a the least significant bit (LSB).

Fig. part (b) illustrates a general problem: We have 4 Δ's representing represented by 5 levels 0…4. A *NoB*=2bit binary input can represent NoL=2^{NoB}=4 levels. Practically we find both solutions to that Problem:

1. Either we subdivide the total output signal range U_R into *L-1* Δ's only,
2. alternatively, we may subdivide range *R* into *NoL* Δ's, but cannot represent either the minimum or the maximum level.

Simple mathematical model: $U_{DACout} = \Delta_{DA} \cdot N_{DACin} + U_{DAoff}$ or generalized

$$\boxed{\boldsymbol{U_{DACout} = \Delta_1 \cdot N_{DACin} + \Delta_0}}$$

where $\Delta_0 = U_{DAoff}$ is the offset and $\Delta_1 = \Delta_{DA}$ the amplification, typically in *V/bit* or *A/bit*.

This chapter about D/A converters will introduce 3 Nyquist-samplers and 3 over-samplers:

1. Equally weighted summation
2. Binary weighted summation
3. R-string
4. PWM: Pulse-width modulation
5. Δ modulation
6. ΔΣ modulation

2.2.1 Equally Weighted Summation

A *DAC* based on equally weighed summation of *M* input bits can represent *L=M+1* levels.

2.2.1.1 Equally Weighted Summation with Thermometric Code

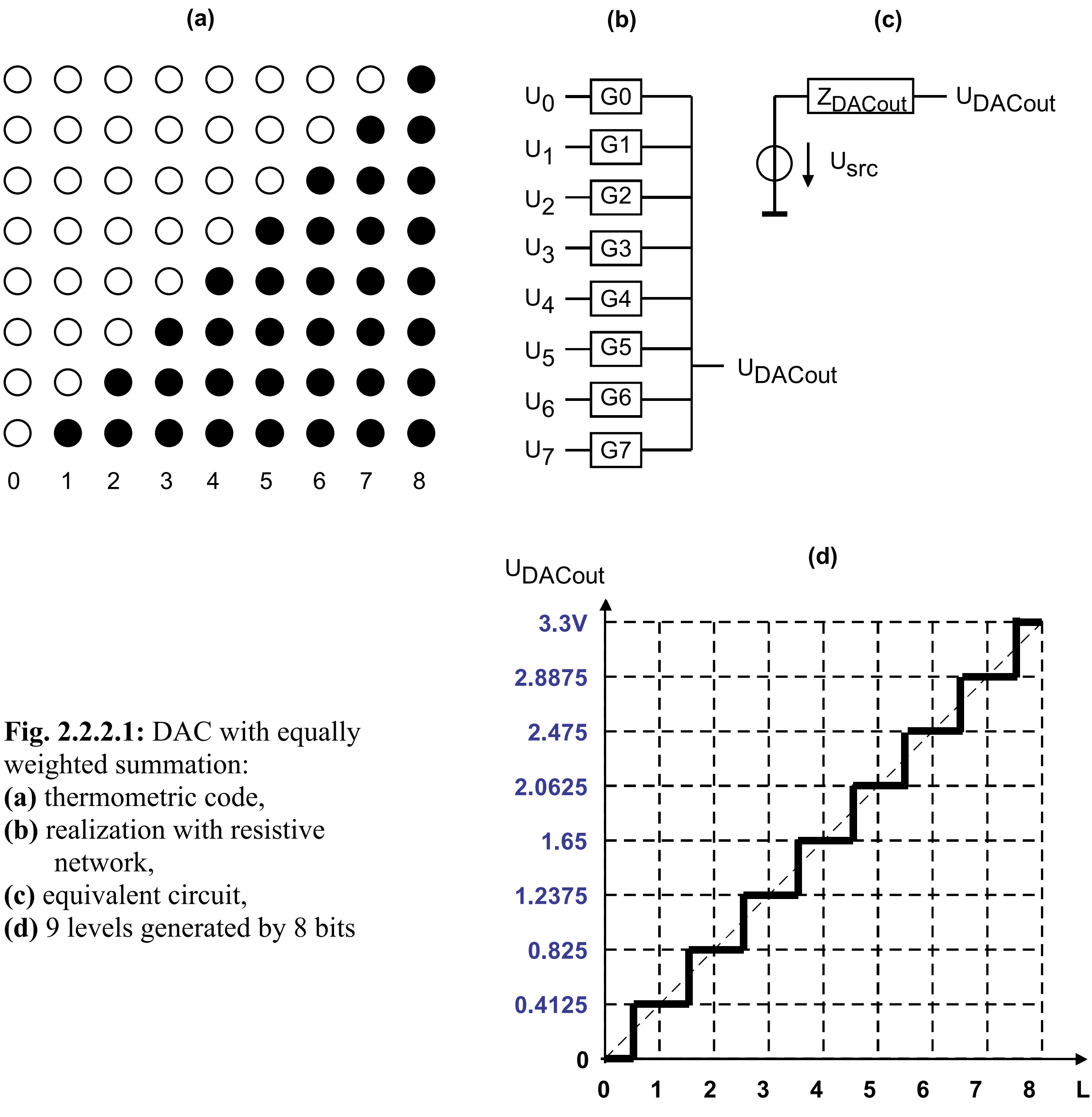


Fig. 2.2.2.1: DAC with equally weighted summation:
(a) thermometric code,
(b) realization with resistive network,
(c) equivalent circuit,
(d) 9 levels generated by 8 bits

The *DAC* in Fig. 2.2.2.1(b) is composed of resistors with value $R_i=1/G_i$, i=1...8. Its output voltage is given by

$$G_{sum} = \sum_{i=0}^{NOB-1} G_i \quad , \quad U_{src} = \sum_{i=0}^{NOB-1} \frac{G_i U_i}{G_{sum}} \tag{2.2.1.1}$$

$$Z_{DACout} = \frac{1}{G_{sum}} \tag{2.2.1.2}$$

The ideal case of $G_i=G_j$ for all $i,j=0...M-1$ and $U_i =$ 0V or U_{max} (typically $U_{max}=V_{CC}$) delivers

$$U_{DACout}(i) = i \cdot \frac{U_{\max}}{L-1}, \quad i=0\ldots L\text{-}1$$

with i being the number of inputs with $U_i=U_{max}$ while all other inputs are 0V. It is seen that the number of Levels being L=M+1 is significantly less than for binary weighted summation. However, as detailed below, we can now repair inaccuracies with digital means.

Example: L=9, U_{max}=3.3V: $U_{DAC,out}(i) = i\cdot\frac{V_{CC}}{L-1} = i\cdot\frac{3.3V}{8} = i\cdot 0.4125\frac{V}{Bit}$, $i=0\ldots 8$.

Practical problems (same as for R2R ladder):

1. The output impedances of the switches (typically MOSFETs) driving the DAC's a_x inputs must be significantly smaller than $2R$, as they add to the respective $2R$-impedances → Choose large impedances for R. Furthermore, larger R consumes lower power.
2. The output load forms a voltage divider with the DAC's output impedance of $Z_{DACout}=R$ → Choose R significantly smaller than the load.
3. The precision of the resistors and switches decides over the accuracy of the DAC.

Point 1 and 2 are contradictory.

2.2.1.2 Equally Weighted Summation with Dynamic Element Matching

Thermometric code fills bits with 1's from bottom to the top. However, there is no need to do so, as only the number of logic-'1' bits is determining for the output level. To compensate for non-matching resistor + switch-impedance combinations $R_i=1/G_i$ we can continuously exchange the inputs that get high/low potential. This presumes oversampling and is called dynamic element matching (DEM).

Dynamic Element Matching (DEM) Using Oversampling

In Fig. 2.2.1.2(a) there is one bit ON, in Fig. part (c) there are 3 bits ON, all the other bits are OFF. Due to the inaccuracies of the resistors, the inner source voltage of the DAC will now generate a pattern as illustrated in Fig. part (d). In other words, if its pattern frequency f_{pat} is sufficiently high, a low pass can remove it. The inaccuracies of the resistors were shifted form frequency f=0 to frequencies $f_{pat}=f_S/M$ and harmonics, where f_S is the sampling frequency and M the number of input bits. This technique is called dynamic element matching or DEM. The resistor-matching problem is solved at low frequencies by DEM. The lower number of levels plus higher sampling speed translates to higher accuracy.

If we do not want to have this "pattern noise" at $f_{pat}=f_S/M$ and harmonics, then we can use an index-randomizer as illustrated in Fig. part (c). It makes the noise white.

It is obvious that this method requires oversampling, i.e. an increased sampling frequency f_S. This matches ideally with other oversampling methods such as ΔΣ modulation.

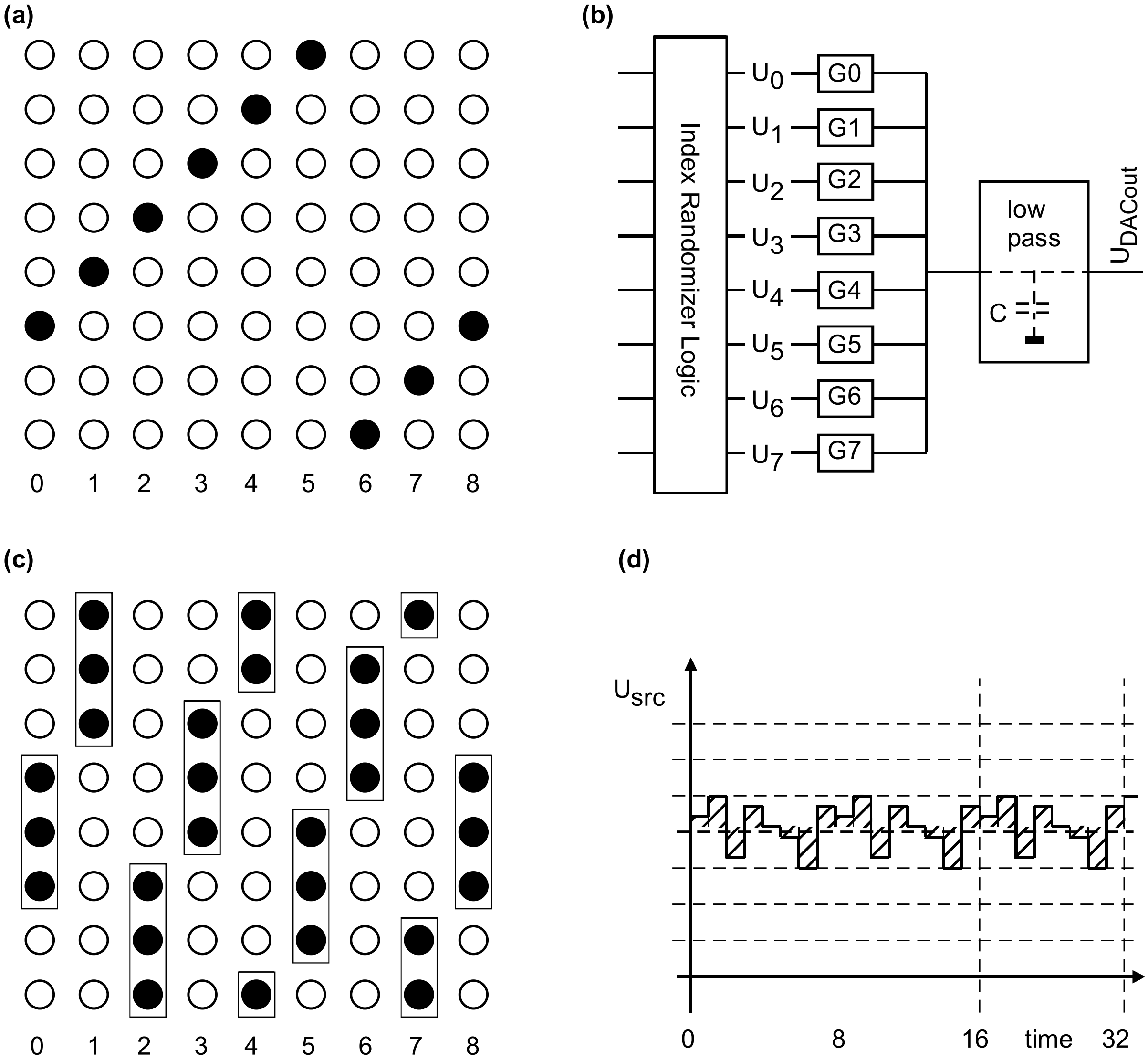


Fig. 2.2.1.2: *DEM* **(a)** rotating coding of 1/8, **(b)** implementing a random logic, **(c)** 3/8 in barrel-shifter coding, **(d)** lower frequencies are generated by the barrel-shifter method.

2.2.2 Binary Weighted Summation

A DAC based on binary weighed summation can represent a number of $NoL = 2^{NoB}$ levels when controlled by NoB bits.

Example: A binary coded unsigned integral number is typically represented as

$a_{M-1}...a_2a_1a_0 = a_{M-1}2^{M-1} + ... + a_2 2^2 + a_1 2^1 + a_0 2^0$ with a_x being 0 or 1.

Example: $11010101 = 1{\cdot}2^7 + 1{\cdot}2^6 + 0{\cdot}2^5 + 1{\cdot}2^4 + 0{\cdot}2^3 + 1{\cdot}2^2 + 0{\cdot}2^1 + 1{\cdot}2^0 = 229_{10}$.

$NoL=2^{NoB}$ numbers can be represented with NoB bits.

2.2.2.1 *R2R* Ladder: *R* and *2R* Resistors Only

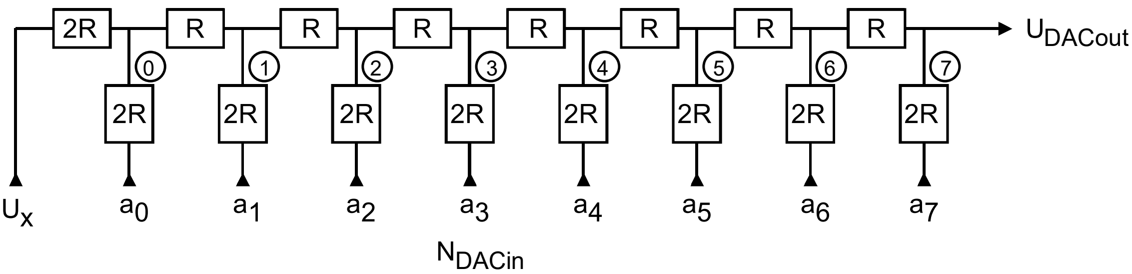


Fig. 2.2.2.1: 8-bit *R2R* DAC realized by an *R2R* ladder.

Fig. 2.2.2.1 illustrates the widely used DAC type using a so-called R2R ladder. (Electrical details how this works are explained e.g. in chapter 1 of script *Schaltungstechnik* of the author [1].) Wires labeled a_x are typically driven either with *gnd*=0V or U_{max}, which is typically V_{CC} supplied by a driver or a digital flipflop. The closer input a_x is to U_{DACout}, the bigger is its impact on it. This DAC works without semiconductors. Such DACs are commercially available.

Its output impedance is

$Z_{DACout} = R$.

This DAC subdivides the voltage range $0...U_{max}$ into $NoL = 2^{NoB}$ Δ's of size $\Delta_{DA} = U_{max}/NoL$. Its output voltage range for NoB controlling bits is

$$U_{DAout} = U_{\max} \sum_{k=0}^{NoB-1} a_k \cdot 2^{k-NoB} + U_{DACoff} \ , \quad a_k = 0 \text{ or } 1 \ \text{ and } \ U_{DAoff} = 2^{-NoB}\, U_x.$$

If U_x in Fig. 2.2.2.1 is connected to *gnd*=0V then U_{off}=0 and U_{DACout} cannot represent the maximum level U_{max}. When $U_x=U_{max}$ then $U_{off}=\Delta_{DA}$ and U_{DACout} cannot represent level *gnd*=0V:

Practical problems:

1. The output impedances of the switches (typically MOSFETs) driving the DAC's a_x inputs must be significantly smaller than $2R$, as they add to the respective $2R$-impedances → Choose large impedances for R. Furthermore, larger R consumes lower power.
2. The output load forms a voltage divider with the DAC's output impedance of Z_{DACout}=R → Choose R significantly smaller than the load.
3. The precision of the resistors and switches decides over the accuracy of the DAC.

Point 1 and 2 are contradictory.

2.2.2.2 Using Binary Graded Component Parameters

The disadvantage of this principle is the need component ratios increasing by a factor 2, which is a considerable problem from a design and accuracy point of view.

For the resistive network as illustrated in Fig. 2.2.2.2 (a) we have with conductor = 1/resistor or $G_\# = 1/R_\#$, we had equations (2.2.1.1) and (2.2.1.2). For the capacitive network as illustrated in Fig. 2.2.2.2 (b), output impedance and output voltage compute as

$$Z_{out}^{-1} = C_{sum} = \sum_{j=0}^{M-1} C_j \quad \text{and} \quad U_{DACout} = \sum_{j=0}^{M-1} \frac{C_j}{C_{sum}} U_j , \qquad (2.2.2.2)$$

respectively. When $U_B = 0$V, the output voltage range is $U_{DACout} = 0 \ldots U_{ref} - 1\ LSB$; when $U_B = U_{ref}$, then the output voltage range is $U_{DACout} = 1\ LSB \ldots U_{ref}$.

(a) Resistive network **(b)** Capacitive network.

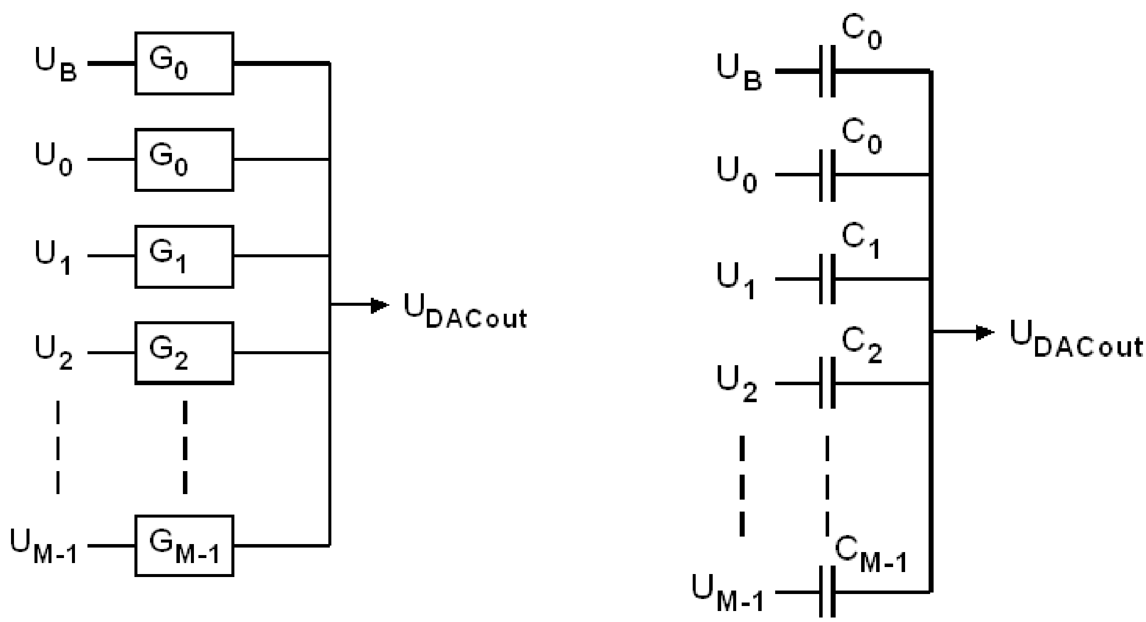


Fig. 2.2.2.2: D/A conversion scheme (among many others) with binary weighted summation

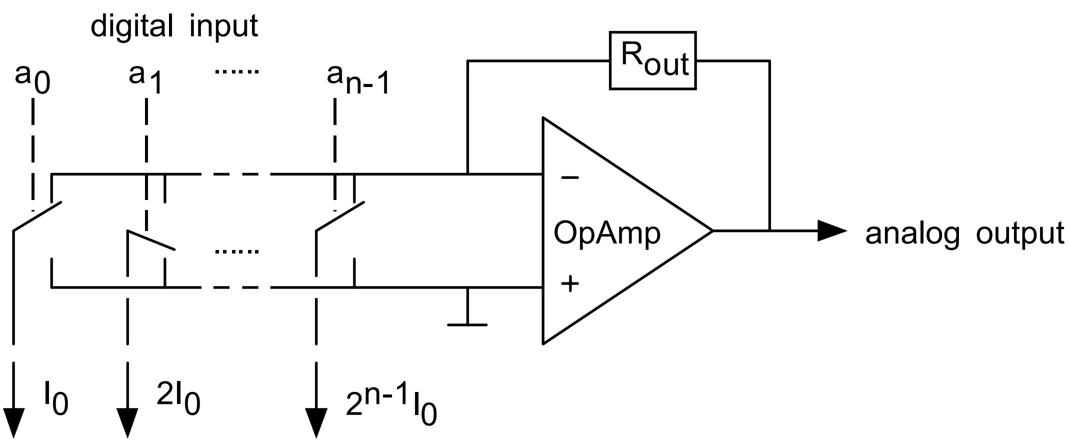
2.2.2.3 Adding Binary Weighted Currents

The disadvantage of this principle is the need of generating current ratios increasing by a factor 2, which is a considerable problem from a design and accuracy point of view.

Greyed out: Optional information, for interested students only

In Fig 2.2.2.3 we add binary increasing currents with binary, whereas Fig. part (a) illustrates the principle: A current is without effect when it is drawn from the virtual ground input of the operational amplifier.

(a) Principle of adding binary weighted currents



(b) Possible realization

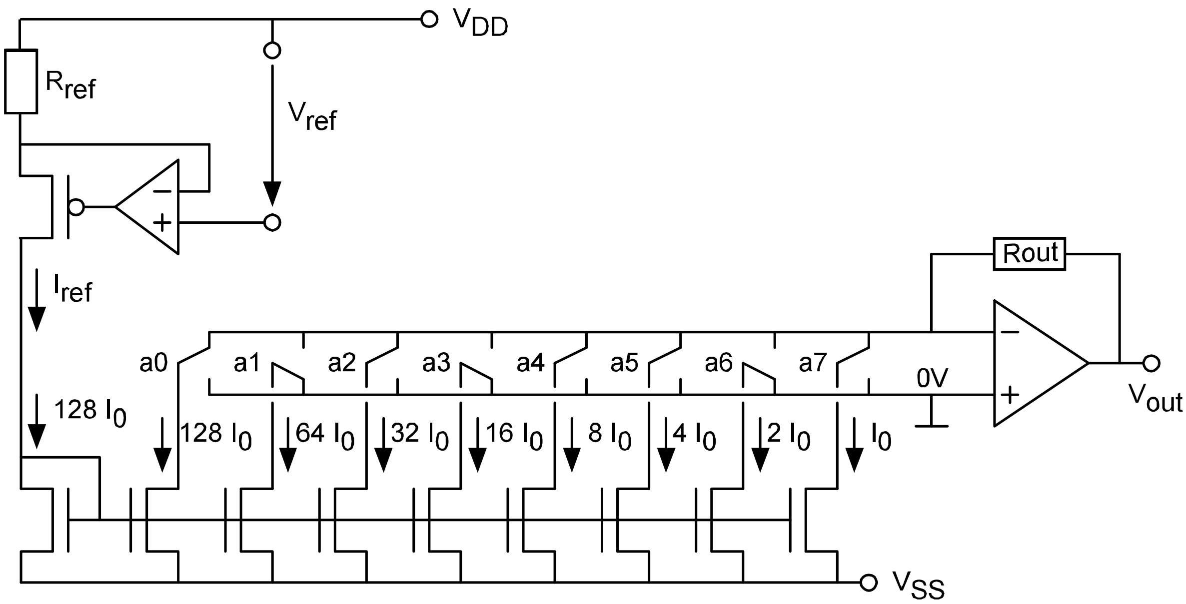


Fig. 2.2.2.3: Summation of currents $I_i=a_i\cdot 2^{i-1}\cdot I_o$ (with $a_i\in\{0,1\}$) and subsequent translation in voltage $U_{DACout}=R_{out}\cdot I_{sum}$.

2.2.3 R - String DAC

R-string DACs a made of a string of resistors of same size, and of an analog multiplexer, that connects one of the node voltages in the string to the output. The analog multiplexer consists mainly of a field effect transistors (FETs) used as switches. Using same-size resistors is technological advantageous, we have no code-inversion or missing codes. However, the node resistance increases to the middle of the chain of resistors forming a RC-lowpass with its capacitive charge. Consequently, the medium output levels have a longer settling time than those near maximum and minimum voltage.

NoB input bits control $NoL=2^{NoB}$ levels from *gnd*=0V to U_{max} (typically $=V_{CC}$). *NoL-1* resistors are required for *NoL-1* possible Δ-steps.

This kind of DAC is particularly found on micro controllers.

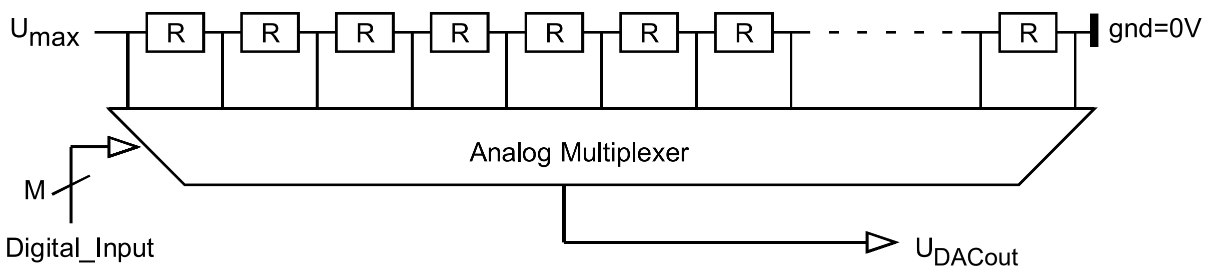


Fig. 2.2.3: R-string DAC (assume *M=NoB*).

Advantages:

- No missing codes or monotonicity problems possible.
- Resistor matching only decides over the accuracy of the inner source voltage (, independently of switches within the analog multiplexer).

Disadvantages:

- Output impedance strongly depends on output voltage.
- Relatively high output impedance maximum.

Exercise:

What is – in the idealized figure above – the minimum and maximum output impedance Z_{out} of the *R*-string? Let U_{max} and $U_{min}=gnd$ be supplied with zero output impedances, assume an even number of N resistors and do not consider the analog multiplexer.

Solutions:

If $U_{out} = U_{max}$ or $U_{out} = U_{min}$ then Z_{out} is theoretically zero. It has a maximum of $Z_{out} = R{\cdot}N/4$ at $U_{out} = ½(U_{max}+U_{min})$.

Rationale: At $U_{out} = ½(U_{max}+U_{min})$ we have a chain of N/2 resistors from output to U_{max} and a chain of N/2 resistors from output to U_{min}. $R{\cdot}N/2$ with $R{\cdot}N/2$ in parallel makes $R{\cdot}N/4$.

2.2.4 Oversampler 1: PWM: Pulse-Width Modulation

2.2.4.1 Benefits of Switching D/A Converters

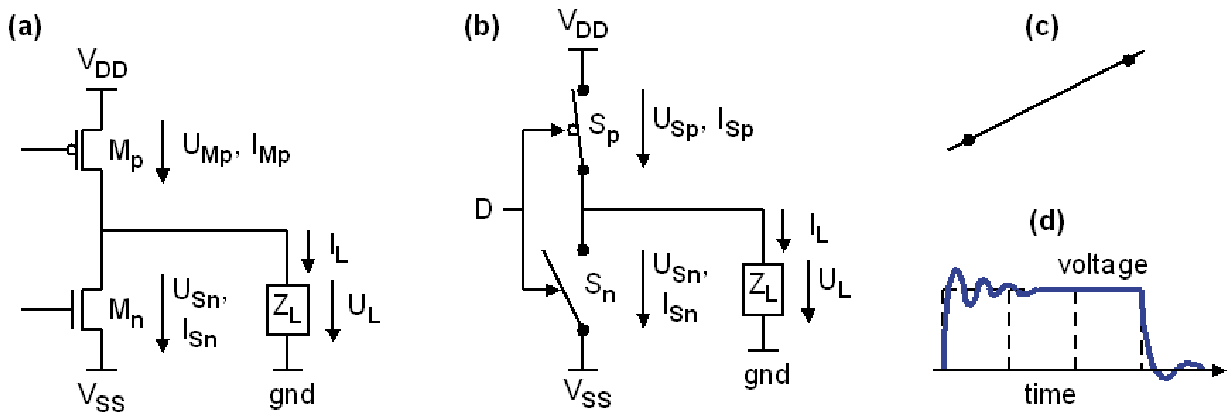


Fig. 2.2.4.1: (a) MOSFETs in half bridge configuration, **(b)** half bridge with ideally 100% efficiency, **(c)** linearity study: a two-level DAC is infinitely linear, **(d)** linearity impairment by signal integrity problems.

The information is transmitted as average value, which makes an averager necessary as demodulator. This averager can be e.g. an electrical lowpass, the mass of a vehicle (car, truck, train,…) or the heat capacity of a room.

Fig. part (a) illustrates a a half bridge using two power MOSFETs as output buffer. Assuming it operated on-switching (i.e. supplying any output voltage) and that the current through MOSFET M_p equals current through the load, i.e. $I_{Mp} = I_L$, the efficiency in the shown situation is $U_L / (U_L+U_{MP})$, which might be significantly less than 50%. The power heating MOSFET M_p is $P_{Mp,loss} = U_{Mp} \cdot I_{Mp}$.

Fig. part (b) illustrates a switching conversion technique that can achieve power efficiencies of theoretically 100%. (Practical >90% is good for low-power / low-voltage applications.) The amount of power heating the switch # (#=p,n) is

$$P_{S\#,loss} = U_{S\#} \cdot I_{S\#} \qquad (2.1.1)$$

with $U_{S\#}$ being voltage across and $I_{S\#}$ current through the switch #. Shown in Fig. part (b) are two switches in positions

Switch S_p closed: $P_{Sp,loss} = U_{Sp} \cdot I_{Sp} = 0V \cdot I_{Sp} = 0\text{W}$
Switch S_n open: $P_{Sn,loss} = U_{Sn} \cdot I_{Sn} = U_{Sn} \cdot 0A = 0\text{W}$

In both cases the switches consume – theoretically - no power. I_S=0A is relatively good approximated in the OFF phase of semiconductor power switches), in the example realized by S_n (except the tail currents of IGBTs). However, U_S at $I_S >> 0\text{A}$ depends on ON resistor R_{ONp} yielding $U_{Sp} = R_{ONp} \cdot$and $P_{Sp,loss} = U_{Sp} \cdot I_{Sp} = R_{ONp} \cdot I^2_{Sp}$. Consequently, low ON resistors $R_{ON\#}$ of the power switches are essential for high efficiency.

The price for high efficiency is a sufficiently fast pulsed signal that must be averaged (demodulated) by a lowpass. This may be for example the mass of a truck, car or train, etc. If an *LC* lowpass could be used as demodulator, then it was lossless on the one hand but oscillating on the other. Practically it will inevitably be an RLC lowpass due to parasitic resistors that must be held as small as possible.

Fig. part (c) illustrates that such two-point switches can be very accurate, theoretically infinitely linear, as a line through 2 points is always infinitely linear.

Fig. part (d) shows that in reality linearity is limited by signal integrity (SI) issues.

2.2.4.2 Analog PWM

- Suitable for analog control
- Advantage: no discrete levels → no limit cylcling problem

2.2.4.3 Digital PWM /DPWM)

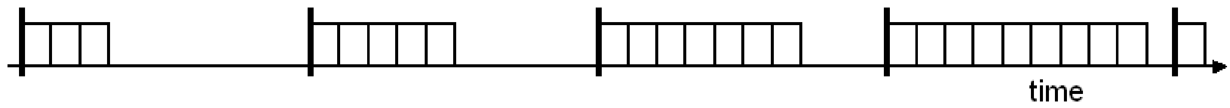


Fig. 2.2.4.3: DPWM Pulses with different widths made of integral multiples of clock cycles

- Suitable for digital control
- Discrete levels → limit cycling problem

Digital Pulse Width Modulation (DPWM) works very similar to equally weighted summation, but the equally weighted signal parts do not appear simultaneously but sequential in time, i.e. one after the other as illustrated in Fig. 2.2.4.3.

The resolution after averaging is limited to a number of $NoL = pwm\_period + 1$ levels, when a pulse-width interval is made up of *pwm_period* bits. In many situations, for example the speed of an electrically powered vehicle, the focus is less on high accuracy than on energy efficiency.

The Digital Pulse-Width Modulator is an oversampling data converter. Demodulator is a lowpass.

2.2.4.4 DPWM Resolution Refinements

Goal: Avoid problems like limit cycling

2.2.5 Oversampler 2: Δ Modulation

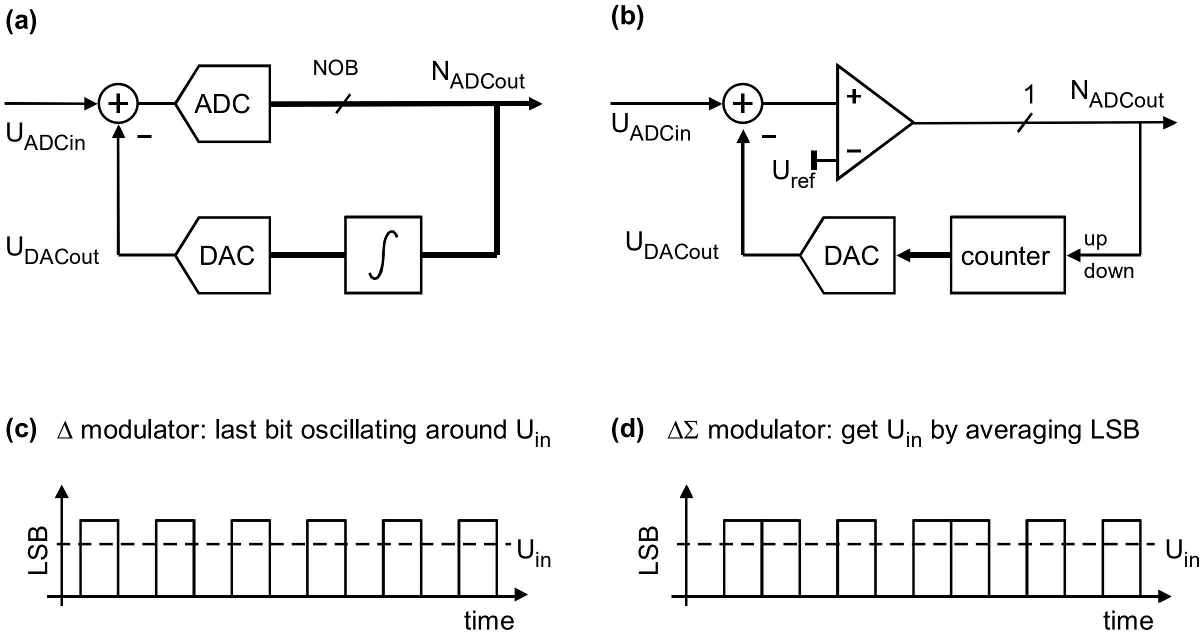


Fig. 2.2.5: Δ modulator: **(a)** schematics, **(b)** realization with 1-bit counter, **(c)** LSB behavior: cannot support DC, **(d)** averaging ΔΣ output yields arbitrary DC accuracy.

The Δ Modulator is an oversampling data converter. Demodulator is an integrator. This converter type was outperformed by ΔΣ modulation.

The Δ-modulator DAC is a modulator/demodulator system. The modulator transfers the signal change only. It has a differentiating characteristic and needs an integrating demodulator.

Fig. 2.2.5(a) illustrates it principle, Fig. part (b) shows a realization for a 1Bit output with an up/down counter as integrator. Fig. part (c) illustrates the behavior of a Δ-modulator's output with U_{DACout} oscillating with its LSB around U_{ADCin}. On the contrary, Fig. part (d) illustrates how the *LSB* of a ΔΣ modulator approaches U_{ADCin} by its average value.

Disadvantages of Δ modulation:
- No DC capability
- Carefully tuned demodulation filter with integrating characteristics required
- Noise shaping = signal shaping, no advantage by noise shaping after demodulation.

This data converter principle was outperformed by ΔΣ modulation, which is superior.

2.2.6 Oversampler 3: ΔΣ Modulation

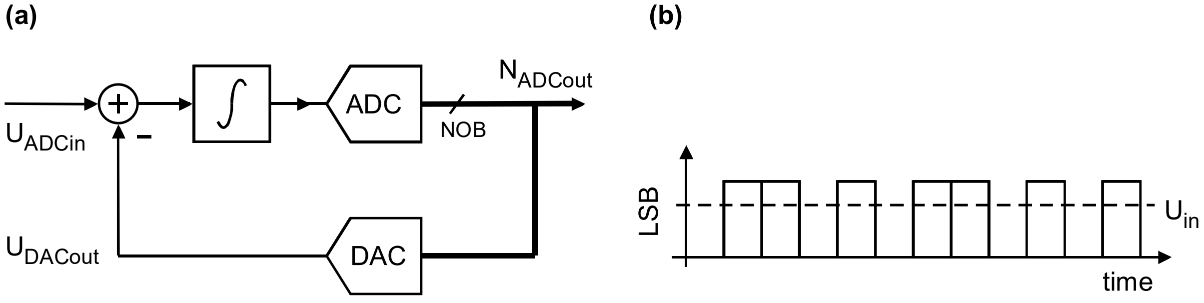


Fig. 2.2.6-1: ΔΣ ADC: **(a)** principle, **(b)** LSB coded to average U_{in}.

The ΔΣ modulator is an oversampling data converter. Demodulator is a lowpass. Advantage: Can obtain extremely high accuracies

A principle of a ΔΣ ADC is illustrated in **Fig. 2.2.6-1:** Translate accuracy to speed exploiting the two main advantages of electronic circuitry: speed a highly precise clock. As the ΔΣ modulator is a loop, it is a question of philosophy what comes first, Δ or Σ. Some people call it ΔΣ modulator, others ΣΔ modulator.

The fundamental principle of ΔΣ modulation is illustrated in **Fig. 2.2.6-2:** Translate accuracy to speed exploiting the two main advantages of electronic circuitry, namely a fast and highly precise clock.

Fig. part (a) shows a digital-to-digital ΔΣ modulation / demodulation system: The modulator translates the digital signal D_0 with bitwidth M_0 and sampling rate f_{S0} into signal D_1 with lower bitwidth $NoB_2 < NoB_0$ and higher sampling rate $f_{S2} > f_{S0}$. The ΔΣ demodulator is a lowpass, here it is a digital one translating the signal D_2 into the lower speed output signal D_1 with increased bitwidth $NoB_1 > NoB_2$ and decreased speed $f_{S1} < f_{S2}$ after down-sampling (also termed *decimation*).

Fig. part (b) shows a ΔΣ ADC, i.e. an analog-to-digital ΔΣ modulation / demodulation system: The modulator runs at high speed to convert the analog signal A_0 into a signal D_1 with low bitwidth NoB_2 (e.g. NoB_2=1 with a comparator as ADC) and high sampling rate f_{S2}. The ΔΣ demodulator in this case is a digital lowpass translating the signal D_2 into output signal D_1 with increased bitwidth $NoB_1 > NoB_2$ and decreased speed $f_{S1} < f_{S2}$. Lowering the bit rate can be dome by ignoring (N-1) out of N samples.

Fig. part (c) shows a ΔΣ DAC, i.e. a digital-to-analog ΔΣ modulation / demodulation system: The modulator translates the digital signal D_0 with bitwidth M_0 and sampling rate f_{S0} into signal D_1 with lower bitwidth $NoB_2 < NoB_0$ and higher sampling rate $f_{S2} > f_{S0}$. A DAC translates D_2 into an analog signal. The ΔΣ demodulator in this case is an analog lowpass translating the roughly quantized analog signal of the DAC into the smooth output signal A_1.

Fig. part (d) shows an industrially very important version of (c): A 1-bit ΔΣ-DAC. Its pseudo-random bit stream is a bit stream controlled such, that it carries the transferred information in its mean value. It can work without analog electronics, can theoretically become infinitely accurate with high oversampling and can realize high efficiency (theoretically 100%) with good switches. Any inertial thing can be the lowpass. It needs no accurate components, because any lowpass (without offset) evaluates accurate mean values from high frequencies, independently from its cut-off frequency.

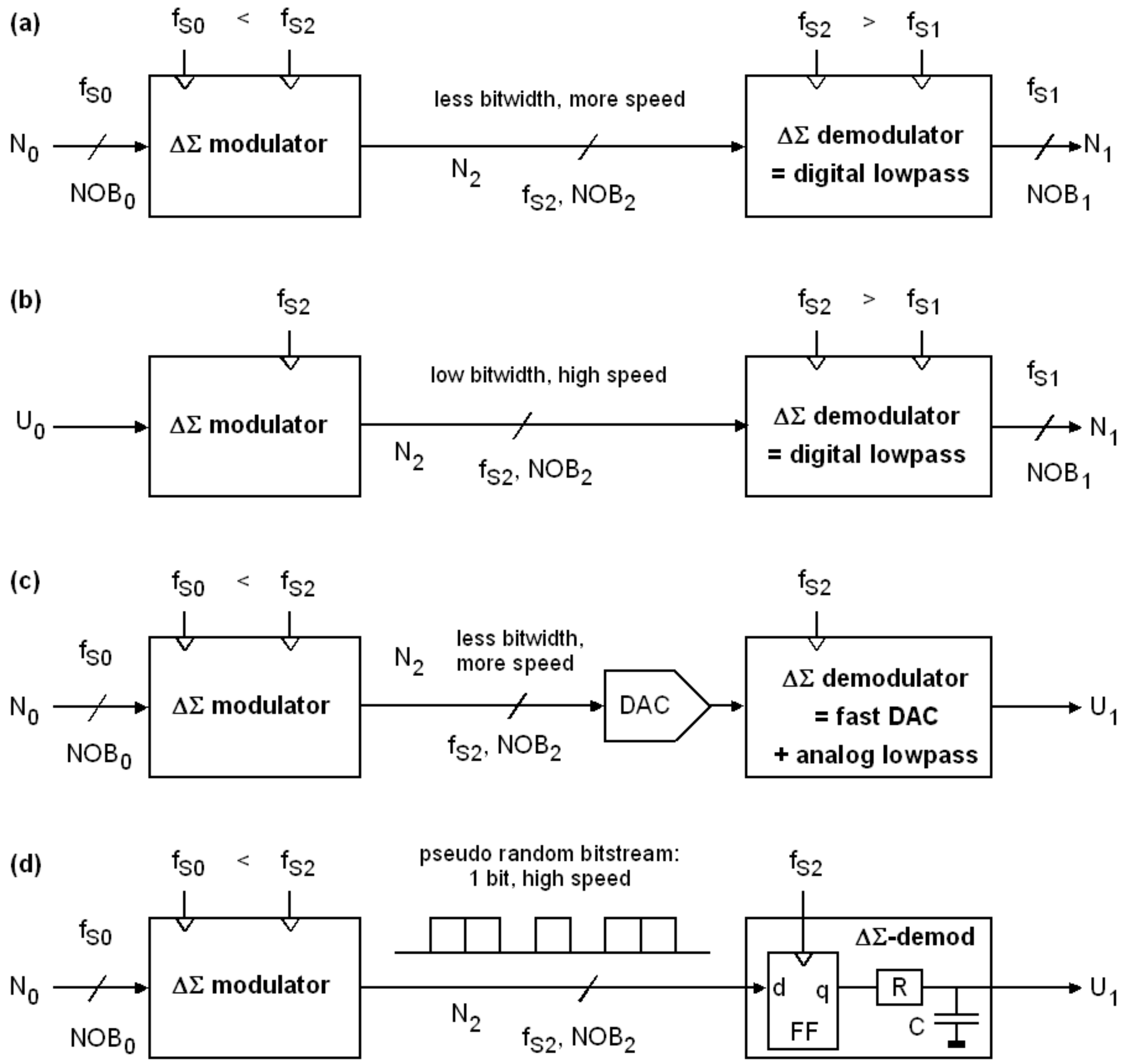


Fig. 2.2.6-2: ΔΣ converters: **(a)** digital to digital, **(b)** analog to digital, **(c), (d)** digital to analog.

Fig. 2.2.6-3(c) shows an example how to connect a little speaker, e.g. of a headphone, to a flipflop. Using both FF-outputs *q* and *qb* doubles the effective output voltage.

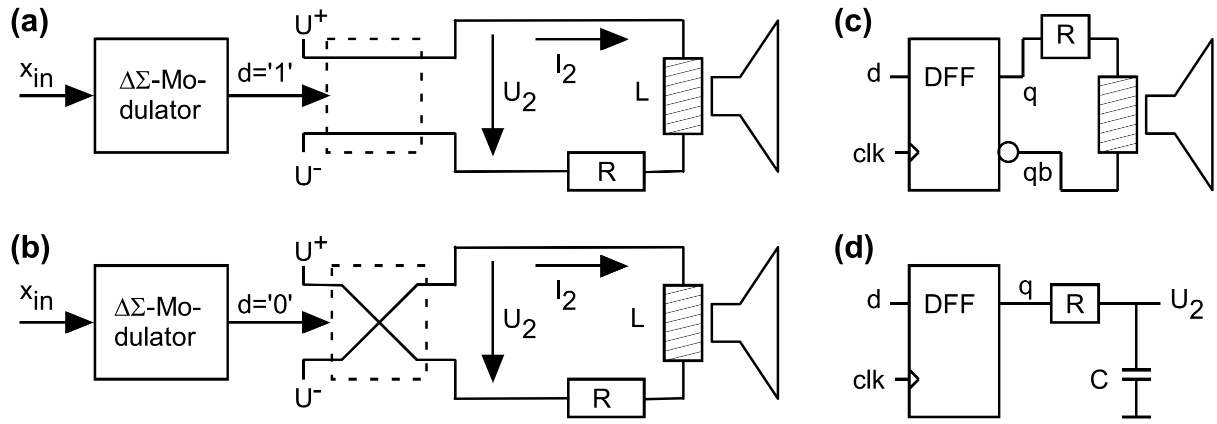


Fig 2.2.6-3: One-bit ΔΣ DAC based on a flipflop: **(d)** is a solution with RC lowpass using one output of the FF while **(c)** doubles the effective output voltage using both *q* and *qb*, **(a)** illustrates the situation of (c) at *d*='1', **(b)** illustrates the situation of (d) at *d*='0'.

Problems:

- High oversampling is required to obtain good accuracy with a 1-bit (= 2-level) DAC.
  Example: A walkman using a 2-level *DAC* delivers sound with a bandwidth f_B=20KHz. according to Nyquist it requires a sampling rate of at least $2f_B$=40KHz. An oversampling ratio (*OSR*) of 100 will require a sampling rate of f_S=4MHz, and *OSR*=1000 requires f_S=40MHz. These sampling speed required for sound are no problem for state of the art electronics.
- The oversampled bits must be delivered with high signal integrity (*SI*), so that all output 1's have same area. Exact rectangular output waveforms are desired. Consequently, we need fast rising and falling edges without voltage overshoot and no noise on the supply rails. (To obtain high *SI*, *Xilinx* offers FPGAs with a particular bank of output FFs having an own supply voltage.)

Summary for the Single-Bit ΔΣ DAC:

- \+ Extremely high efficiencies obtainable, close to 100%
- \+ High accuracies obtainable by high oversampling rates
- \+ Independent of the lowpass-devices accuracy,
- \+ Lowpass can be any integrating device (electrical, mechanical, thermal cap., mass,..)
- \+ Cheep to build: no analog devices required.
- \+ 2-level DAC is always linear (a line through 2 points is always linear), but
- \- Requires high oversampling ratio and
- \- high signal integrity,
- \- is not appropriate for power electronics

2.3 Analog-to-Digital Converters (ADCs)

This chapter about A/D converters will introduce 3 Nyquist-samplers and 3 over-samplers:

1. ADCs based on a successive approximation register (SAR)
2. Flash and Semi-Flash converters
3. Pipelined ADCs,
4. PWM: Pulse-width modulation
5. Δ modulation
6. ΔΣ modulation

Amplification: $\boldsymbol{\alpha_1 = 1/\Delta_{AD}}$ **in *bit* / V (or other quantity as V, e.g. A, °K, ...)**

typically measured in *bit/V, bit/A, bit/°C, bit/meter*,... An ADC followed by a DAC, with Δ_{AD} and Δ_{DA} being the respective smalles voltage steps, has the amplification

$$ada = \alpha_1 \cdot \Delta_1 = \frac{\Delta_{DA}}{\Delta_{AD}}$$

Throughput is measured in *KSPS* or *MSPS* (kilo or mega samples per second, respectively), which is the frequency of digital output sample delivery. Delay τ_{delay} is the time elapsed from sampling an analog input quantity to delivering the respective digital output value.

An ADC is always based on a *DAC* as sub-component and cannot be better than this DAC.

Simple math. ADC model: $N_{ADCout} = round\left(\frac{U_{ADCin} - U_{ADoff}}{\Delta_{AD}}\right) = round\left(\alpha_1 \cdot U_{ADCin} + \alpha_0\right)$

The ADC generates a quantization error, e_q, mathematically modeled as round-off error as illustrated in Fig. 2.3.0-2.

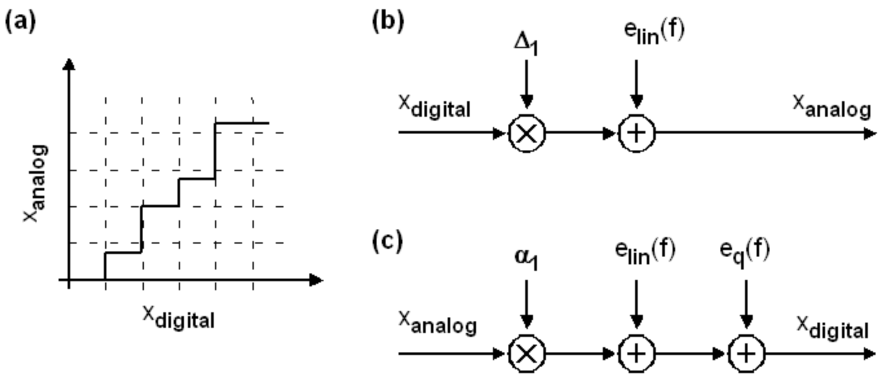


Fig. 2.3.0-1:
(a) A/D und D/A conversion generates linearity errors
(b) DAC and
(c) ADC behavioral models from signal processing view

Quantization noise $\boldsymbol{e_q(t)}$ is generated by ADCs only, not by DACs.

The digital-to-analog converter (DAC) can be modeled according to Fig. 2.3.0-1(b) as linearity error and amplification Δ_1, e.g. in *V/bit*. **A DAC does not generate quantization noise** as it translates *NoL* digital levels into *NoL* analog levels.

The analog-to-digital converter (ADC) can be modeled according to Fig. 2.3.0-1(c) as linearity error and amplification $\alpha_I \approx 1/\Delta_{AD}$., e.g. in *bit*/*V*. **An ADC generates quantization noise** as it translates an infinite number of analog input levels to *L* digital levels, as sketched in Fig. 2.3.0-2. More detailed insight into quantization noise will e presented in chapter 4.

(a) Setup to measure A/D and D/A conversion characteristics.

(b) Ideal quantization.

(c) Quantization noise $e_q = U_{ADCin} - U_{DACout}$

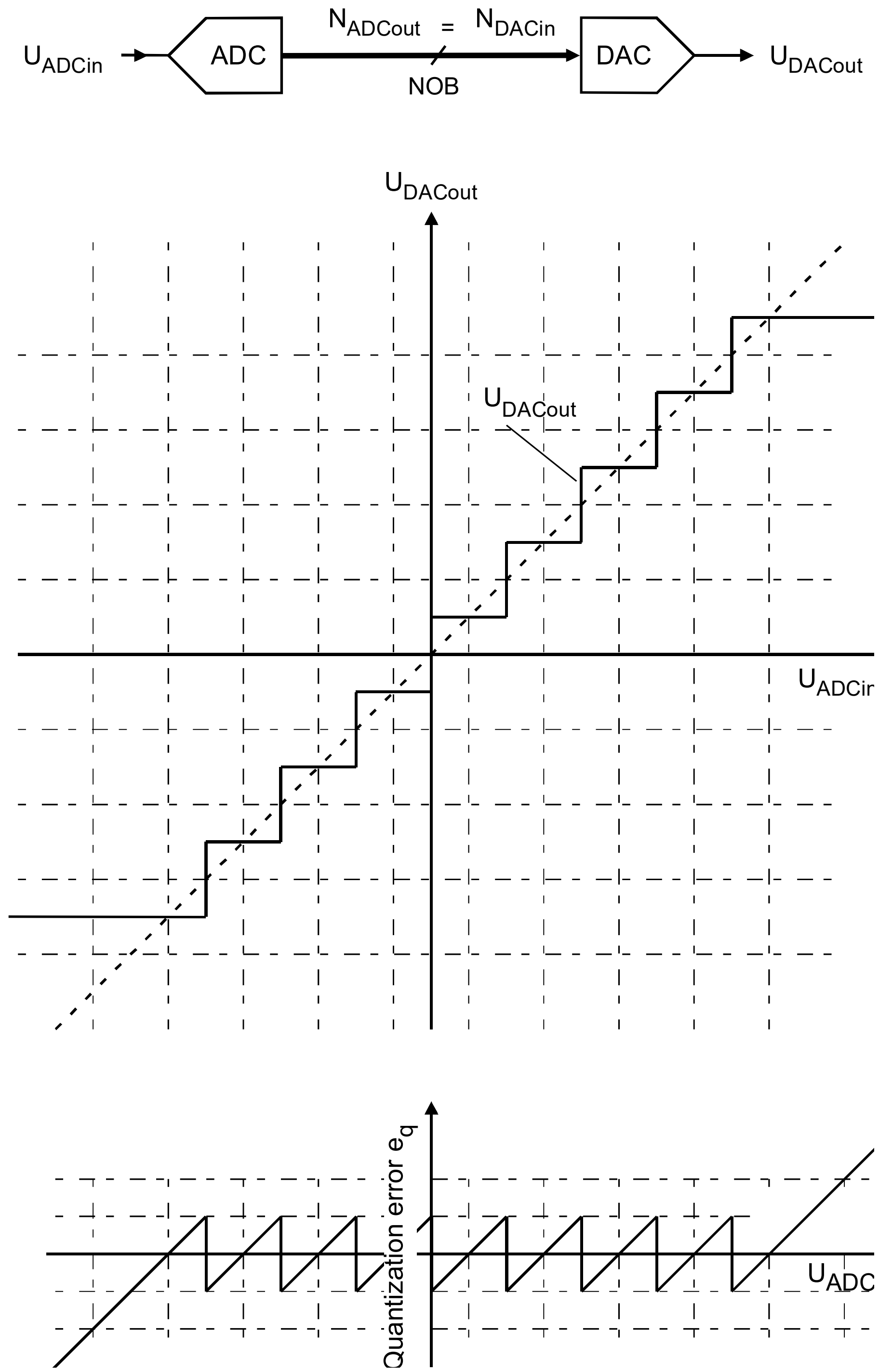


Fig. 2.3.0-2

2.3.1 Successive Approximation Register (SAR) ADC

This is the most probably mostly used ADC type due to its good price/performance relationship. The acronym SAR stands for "successive approximation register", which is contained in the successive logic. The conversion process of this ADC type is illustrated in Fig. 2.3.1:

1. Initialize: successive logic sets j to its maximum value j=NoB-1 (pointing to the MSB), with NoB standing for "Number of Bits".
2. (a) leave a_k unchanged for $k>j$, set a_j='1', set a_i='0' for $i<j$, evaluate U_{DACout} .
   (b) If $U_{DACout} > U_{in}$ set a_i to '0', decrement j, go to (a).
3. If j=0 go to 1.

- In practical applications, there is no phase (b) as illustrated for educational purposes in the graphics below. Resetting a_j and setting a_{j-1} can be made at the same time.
- This kind of ADC will always yield to keep $U_{DACout} \leq U_{ADCin}$ yielding a quantization error offset of -Δ/2 as illustrated in Fig. 2.3.0-2.
-

(a) Architecture of a SAR ADC using a DAC in the feedback branch.

(b) Conversion process: approximate $U_{DAC,out}$ to $U_{ADC,in}$ by trial and error from most to least significant bit

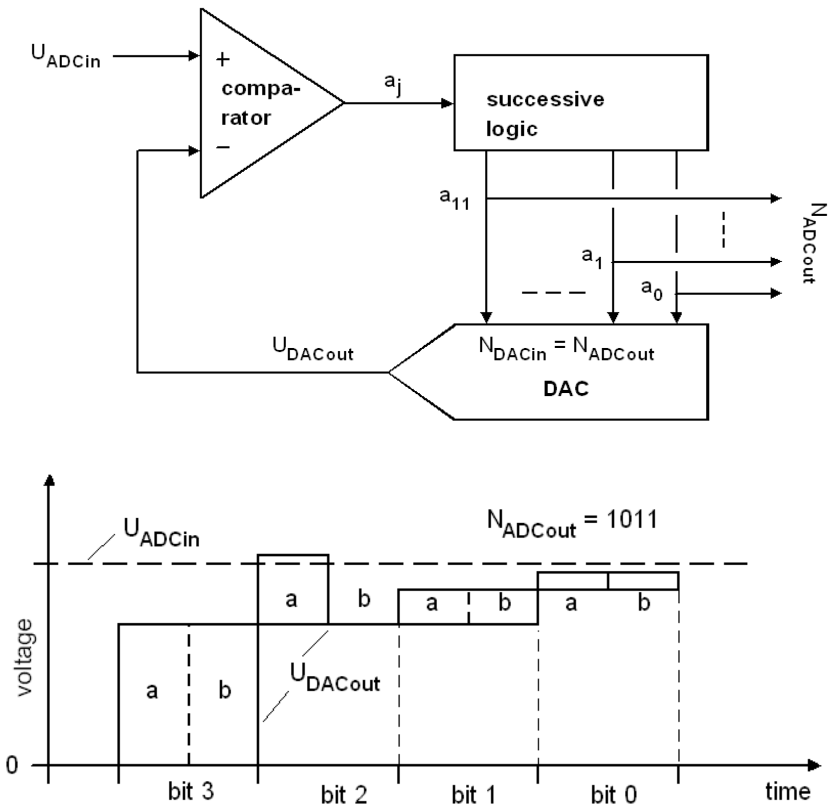


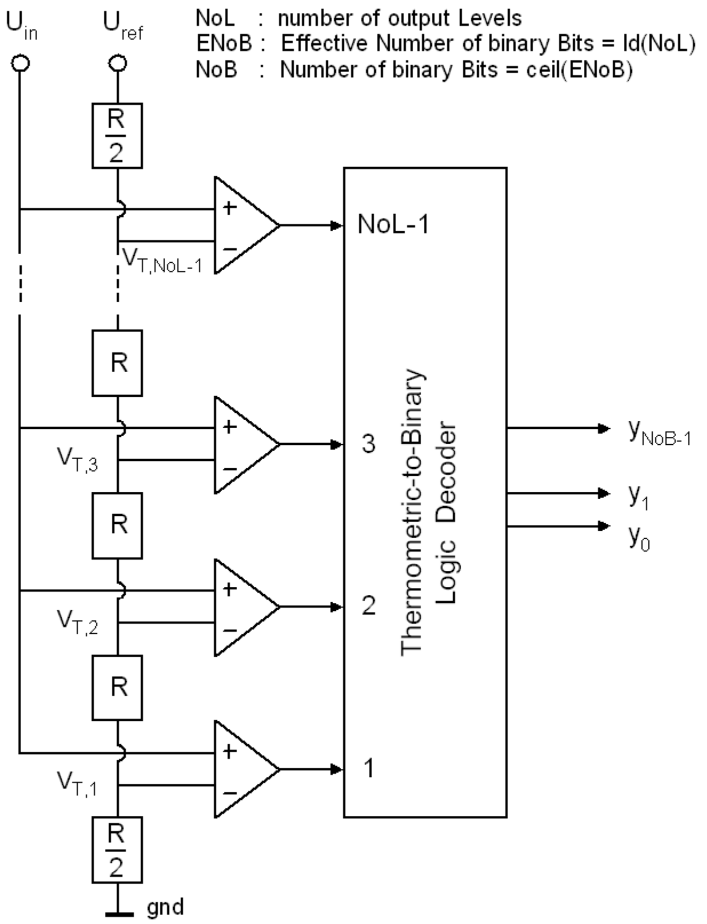
Fig. 2.3.1: Principle of successive approximation register (SAR) A/D conversion

2.3.2 Flash and Semi-Flash ADC

2.3.2.1 Flash ADC

Fig. 2.3.2.1

(a) Schematic:
NoL level flash ADC architecture,



(b) Computing thresholds:

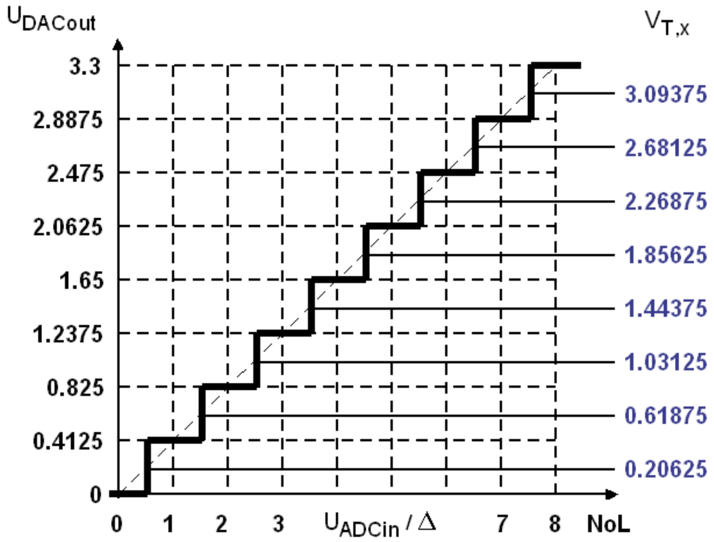
Remember: *NoL* level DAC output voltage formula:

$$U_{DACout} = \frac{i}{NoL-1} V_{CC}\ ,\ i=0...NoL\text{-}1$$

Thresholds are given by

$$V_{T,j} = \frac{j-0.5}{NoL-1} U_{ref}\ ,\ j=1...NoL\text{-}1$$

This example uses $NoL = 9$ and $U_{ref} = 3.3$V as example.



Note that the Flash ADC has no feedback loop. This makes it fast; the result can be obtained within 1 clock cycle (therefore "flash"). Also the flash ADC contains a DAC, namely an *R*-string DAC to generate the thresholds $V_{T,i}$ with U_{ref} being typically V_{CC}.

The flash-DAC generates thermometric code, ideal to drive a DAC with equally weighted bits. Due to offsets of the comparators, we might have missing bits in the thermometric code. This problem can be overcome by using a simple adder a decoder logic.

Advantages of the flash ADC:
+ fast (1 cycle),
+ no DAC in the feedback loop.

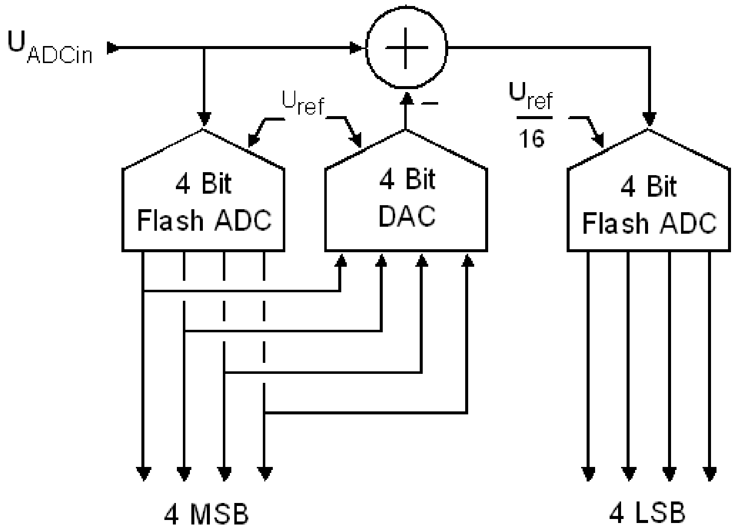
Disadvantages of the flash ADC:
- requires *NoL*-1 comparators for *NoL* levels,
- consequently low resolution (typ.: 4...8 bit)

Example: To obtain *NoB*=4 binary bits corresponding to $NoL=2^{NOB}$=16 levels we need *NoL*-1=15 comparators. For an *NoB*=8 bit flash ADC featuring $NoL=2^{NoB}$ = 256 levels we need 2^{NOB}-1=255 comparators.

Example:
Maxim, "*MAX104: ±5V, 1Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier*", available: https://datasheets.maximintegrated.com/en/ds/MAX104.pdf

2.3.2.2 Semi-Flash ADC

(a) with two different reference voltages.



(b) with single reference voltage and multiplier.

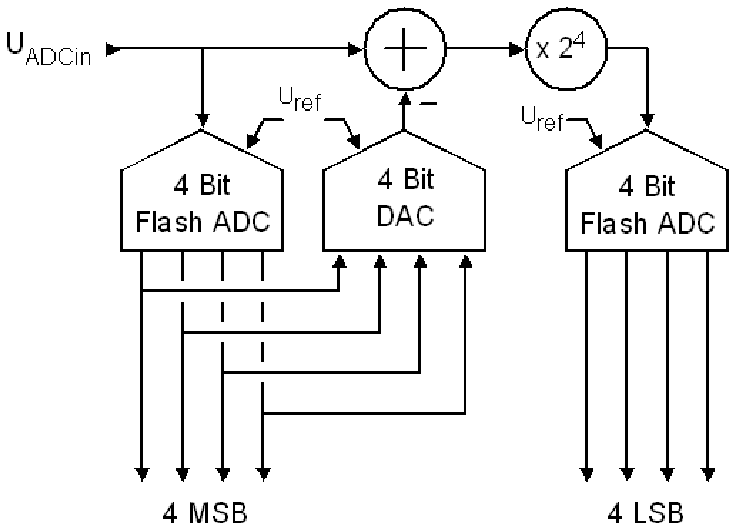


Fig. 2.3.2.2: Semi-flash ADC made of two 4-bit flash ADCs

Advantages of the semi-flash ADC:
+ still quite fast (1 cycles),
+ no DAC in feedback loop.

Disadvantages of the semi-flash ADC:
- requires fewer comparators than the flash ADC, but still many,
- medium resolution (typical 8...12 bit)

2.3.3 Pipelined-ADC

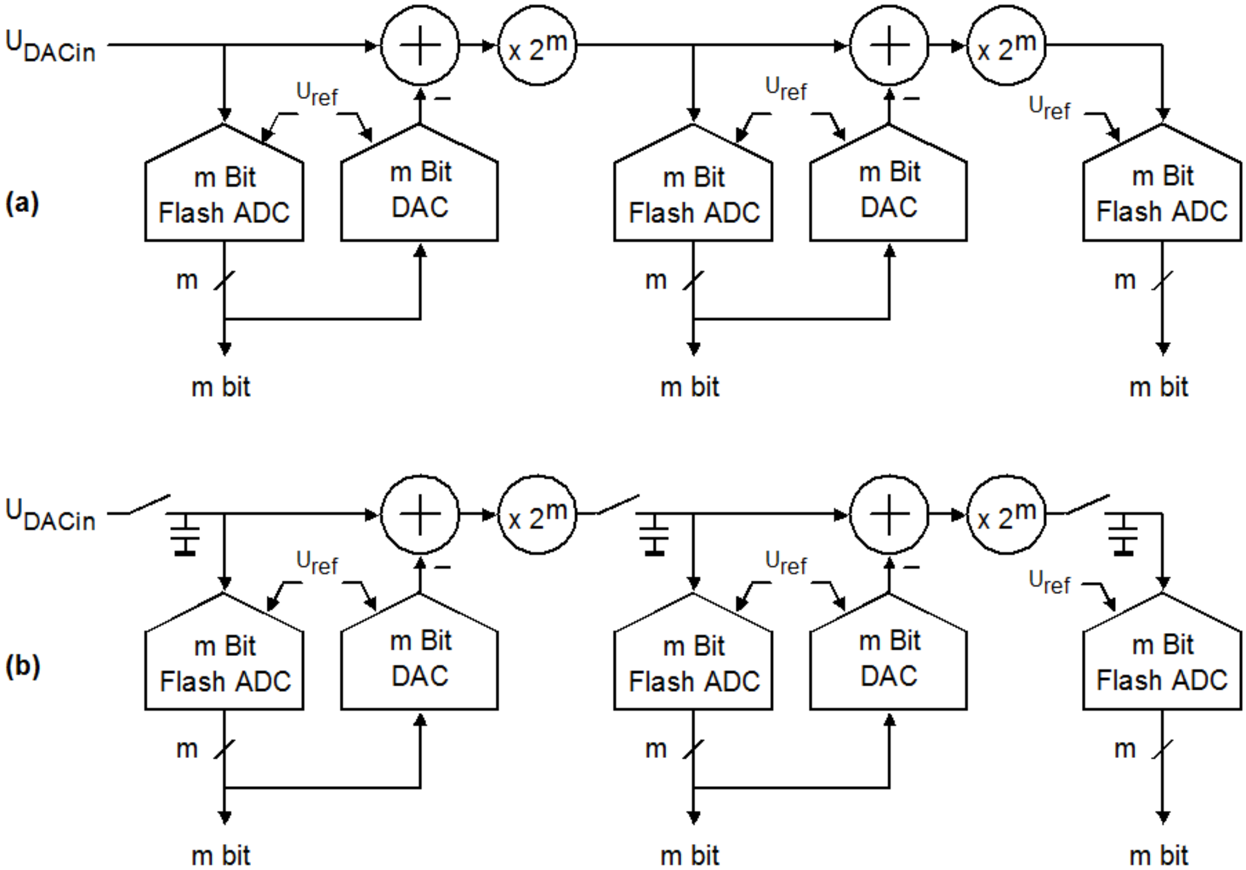


Fig. 2.3.3-1: (a) Three-stage semi-flash ADC, **(b)** three-stage pipelined ADC

Fig. 2.3.3-1(a) shows a three-stage semi-flash ADC which gets slower with an increasing number of stages. The same clock frequency like a flash ADC is obtained with a pipelined ADC by using sample & hold elements between the stages.

Now we have to distinguish between throughput in samples/second and the time delay from taking the first sample to the output of the digital value.

Correction bits as seen in Figs. 2.3.3-2 and -3: There are sophisticated techniques to compensate for non-ideal components. Particularly a method using a Redundant Signed Digit (RSD), which was originally developed for binary division [Hws79] and later rediscovered for ADCs [Hwa79], [GJV92], [MJ94], [HBP96], [KG95], [RG95], [WW99] delivers an important contribution for the accuracy of pipelined ADCs.

Cyclic ADC:
If we do not have N stages but use the same stage N times, then we call this a cyclic ADC. It consumes less chip area on the cost of less throughput. The difference to SAR is small and preferably given by the sample & hold circuit [IK2000].

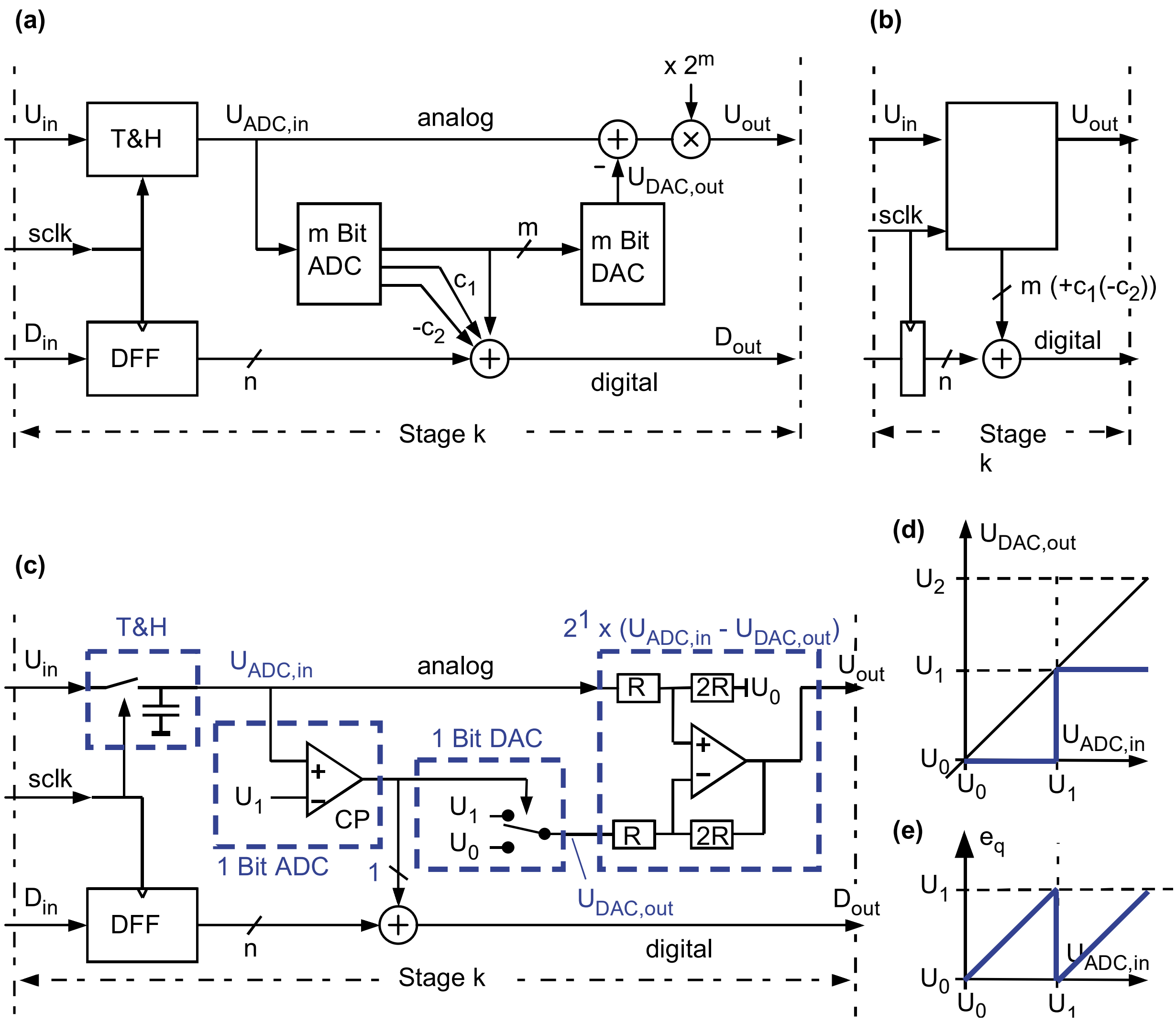


Fig. 2.3.3-2: **(a)** stage of pipelined-ADC, **(b)** stage of pipelined-ADC, higher level, **(c)** stage with 1-bit flash, **(d)** electrical characteristics of 1-bit flash stage.

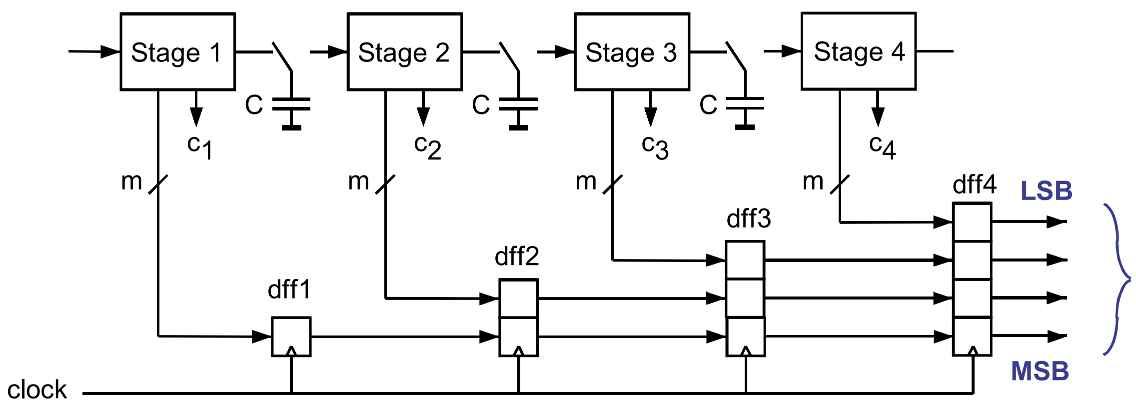


Fig. 2.3.3-3: Four-stage Pipelined-ADC with m bit per stage, correction bits unused.

2.3.4 Oversampler 1: PWM ADC

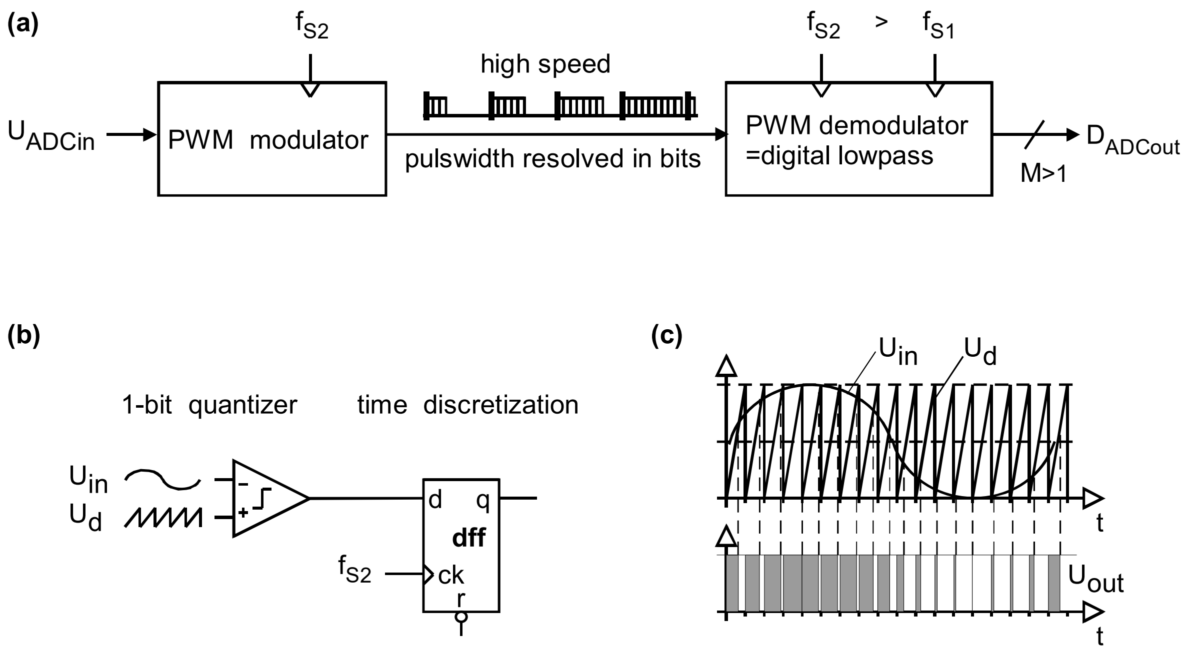


Fig. 2.3.4: PWM-ADC: (a) complete system consisting of modulator and demodulator, the latter being a lowpass, (b) respective circuitry and (c) waveforms of (b).

Demodulator is a lowpass.

Pulse-width modulation is easy to realize as shown in Fig. 6.1.1.5. Demodulator is a lowpass like similar like for ΔΣ modulation. Accuracies to be obtained are minor to ΔΣ modulation, but PWM is more suitable for switching high currents due to less switching events.

Superior to ΔΣ when the number of switching events must be minimized.

2.3.5 Oversampler 2: Delta-ADC

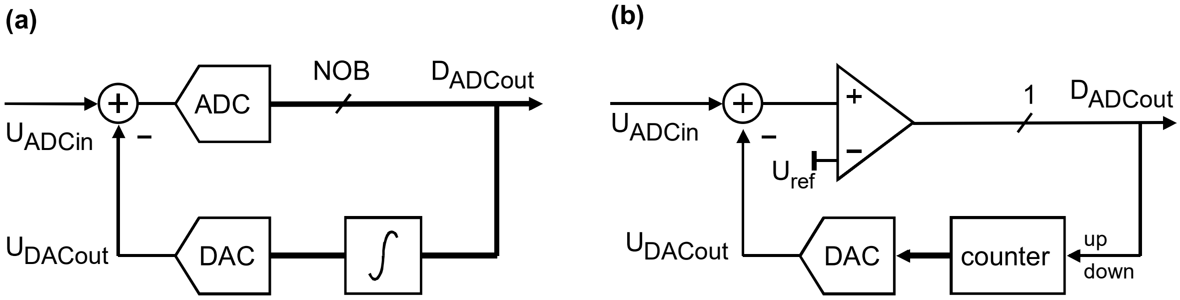


Fig. 2.3.5: Δ-ADC: **(a)** Principle: Integrator in feedback loop, **(b)** 1-bit realization, counter = int.

Transfers change of signal (= delta) only.
Incapable of transmitting DC values
Has an integrator in the feedback loop
Consequently, STF is a differentiator (inverse of integrator)
Demodulator must obtain be an Integrator
Was replaced by ΔΣ modulator.

Fig. 2.3.5(a) illustrates the basic principle of transmitting the signal change only, using an integrator in the feedback branch. The DAC is controlled such, that U_{DACout} follows U_{ADCin} as close as possible.

Fig. 2.3.5(b) illustrates a realization with a comparator as 1-bit quantizer. The integrator is frequently realized as counter using the output bit an up/down control signal.

Disadvantages: same as for -> Δ DAC

This data converter type was replaced by the ΔΣ modulator, which is superior.

2.3.6 Oversampler 3: Sigma-Delta-ADC

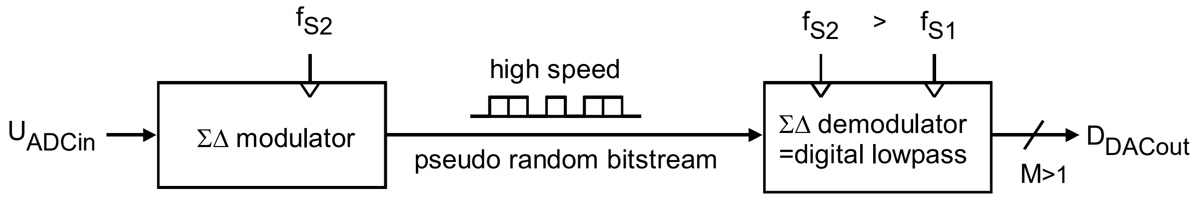


Fig. 2.3.6: ΣΔ-ADC.

Demodulator is a lowpass.

The ΔΣ ADC was already sketched in Fig. 2.2.6-1(b). It translates an analog quantity into a low-resolution data stream. 1-bit pseudo-random bit-streams are possible but significantly different to PWM. Bits do not come in blocks and noise shaping techniques code significantly more accurate results after demodulation than PWM. (This topic will be discussed later in more detail.)

The need for oversampling rises often from the need to avoid analog anti-aliasing filtering. Thus, lowpass anti-aliasing filtering is shifted from the analog to the digital domain.

Comment:
Some people say that the ΔΣ modulator is slow. That is not true: the modulator is fast, but the demodulating lowpass filter might have a significant settling time. ΔΣ ADCs are typically relatively energy intensive, as massive digital filtering at high clock speeds does also cause increased energy consumption.

2.3.7 Special ADCs

2.3.7.1 Windowed ADCs

2.3.7.2 Delay-Line-Based ADC

2.4 Features and Quality Criteria

In former times the figure of merit (Q) for A/D and D/A converter is the product of speed and accuracy. With Δ corresponding to a minimum step and τdelay the time span between input sampling and output sample available.

Quality Criterion 1: $Q_1 = \dfrac{1}{\Delta \cdot \tau_{delay}}$ e.g. in $\left[\dfrac{1}{Vs}\right]$

With pipelined ADCs we had to decide wht delay is meant: the delay from input to output sample or the the inverse of the throughput:

Quality Criterion 2: $Q_2 = \dfrac{samples/\sec ond}{\Delta}$ e.g. in $\left[\dfrac{samples}{Vs}\right]$

It depends on the situation what is more important: A video camera writing data to a memory needs throughput, a fast control loop requiring immediate reaction may prefer I→O delay. Today, we have tohter criteria to evaluate A/D and D/A data converters.

Some acronyms frequently found in the literature, e.g. [RO2007]

DNL	Differential Non-Linearity
INL	Integral Non-Linearity (maximum deviation from ideal characteristic)
Monotonicity	is the curve monotonously or strictly monotonously rising or falling?
Thoughput and Delay	measured in samples per second
KSPS, KS/s	Kilo samples per second
MSPS, MS/s	Mega samples per second
GSPS, GS/s	Giga samples per second
SNR	Signal to Noise Ratio
SFDR	Spurious Free Dynamic Range
THD	Total Harmonic Distortion (German: Klirrfaktor)
SINAD, SNDR, S/(N+D), THD+N:	Signal to Noise and Distortion Ratio
ENOB	Effective Number of Bits

2.4.1 DNL and INL (Static)

Differential non-linearity specifies the maximum difference of two neighboring steps. If it is given as relative value (e.g. in %) we must specify: relative to what? Let's assume of an ideal Δ.

DNL $= \dfrac{\Delta_n - \Delta_{n-1}}{\Delta_{ideal}}$, typically given in %.

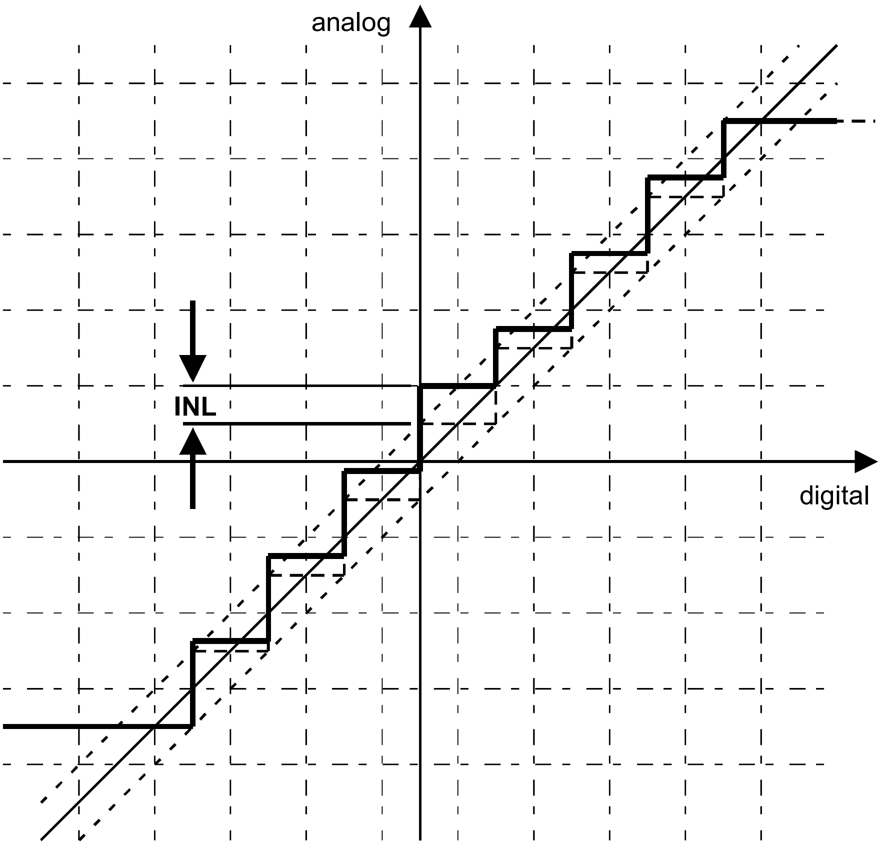
Integral non-linearity specifies the maximum difference to the ideal conversion line. It is typicall specified in % or relative to a least significan step (Δ).

INL: maximum total deviation from the ideal curve.

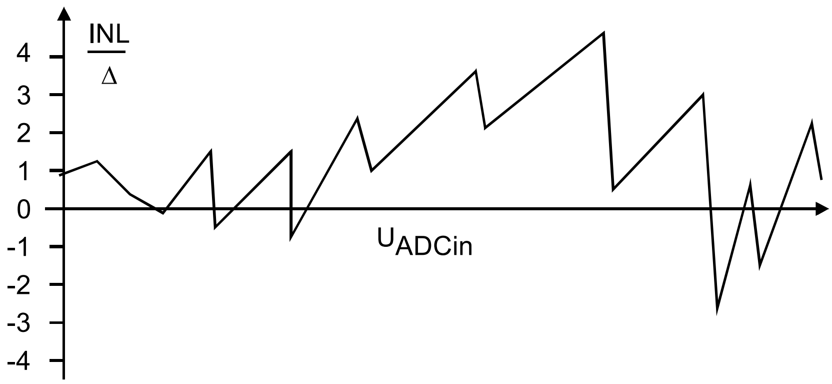
More detailed information on measuring DNL and INL can be found e.g. at Maxim Integrated: "*INL/DNL Measurements for High-Speed Analog-to-Digital Converters (ADCs)*", available: https://www.maximintegrated.com/en/app-notes/index.mvp/id/283.

Fig. 2.4.1

(a) DNL (differential non-linearity) describes the maximum difference of two neighboringΔ's, INL (integral non-linearity) describes the maximum deviation from the ideal curve.



(b) INL plots like this are typically found in the literature, e.g. [ZA2005].



2.4.2 Monotonicity (Static)

Mathematics:

- A curve is monotonously rising or falling if its slope is ≥0 or ≤0, repectively.
- A curve is strictly monotonously rising or falling if its slope is >0 or <0, repectively.

Missing Codes: Some bits cannot be represented. Example an ADC delivers output values 0 1 2 2 2 5 6 7 instead of 0 1 2 3 4 5 6 7. From a mathematical point of view it is monotonously but not strictly monotonously. For SAR-ADCs, this problem typical typically occurs for too high clock speeds.

Monotonicity: Monotonicity error include slope changes. A data converter may feature errors like delivering 0 1 2 3 2 5 6 7 instead of 0 1 2 3 4 5 6 7.

2.4.3 Delay and Throughput

Delay (τ_{delay}) is the time span between input signal spampling and availability of the converted output value.

Thoughput is the number of samples per second deliverd at the output. It is measured in KSPS, MSPS or GSPS. For many converters like SAR ADC we find *throughput* = $1/\tau_{delay}$. Particularly for pipelined converters we have *throughput* >> $1/\tau_{delay}$..

2.4.4 SNR: Signal to Noise Ratio

Signal to Noise Ratio: $SNR = \frac{P_{Signal}}{P_{Noise}} = \frac{A^2_{Signal}}{A^2_{Noise}}$ for any curve.

Matlab function $R = snr(x,e)$ assumes x to be a vector of signal samples e a vector of error (noise) samples. With number of samples being *NoS* = *length(x)* == *length(e)* Matlab computes

$$SNR = snr(x,e) \quad \Leftrightarrow \quad SNR = \frac{\sum_{n=1}^{NoS} x_n^2}{\sum_{n=1}^{NoS} e_n^2}$$

2.4.5 *SFDR* Spurious Free Dynamic Range

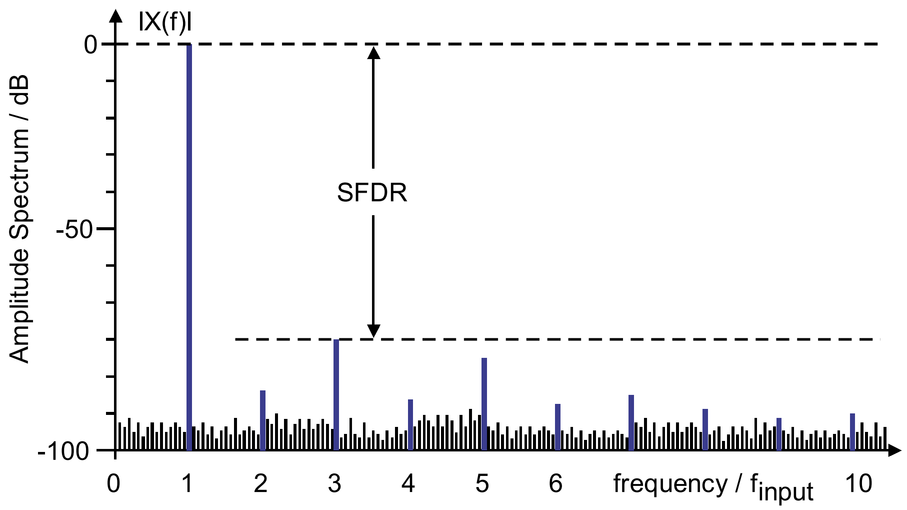
SFDR computes a maximum distortion, characterized by fundamental wave at maximum sinusoidal shape und maximal harmonic.

For measurement of the „spurious free dynamic range“ (SFDR) we feed a sinusoidal wave (e.g. 1KHz) into the system and observe the *Fourier* transform of the output signal: The difference between the amplitude of the input signal (which is by definition 0 dBc) and the highest harmonic is the *SFDR*.

$$SFDR = \frac{P_{Signal}}{P_{\max.harmonic}}, \qquad THD_{dB} = 10dB \cdot \log\left(\frac{|X(f_1)|^2}{\max\left\{|X(f_k)|^2\right\}}\right) \quad \text{with } k > 1 \text{ and } \quad f_k = k \cdot f_1,$$

To not measure the quality of the signal generator but the quality of the system under test: Measure both input and output signal and make sure that the quality of the input signal is sufficiently better than the quality of the output signal. “Sufficiently” depends on accuracy.

Fig 2.4.4: Definition of *SFDR*. Typical measurement of spectrum analyzer, acc. to [ZA2005]. It is seen that there is noise at any frequency, plus harmonics of the test signal frequency. In the example we see some 80dB *SFDR*.



2.4.6 *THD*: Total Harmonic Distortion

The Total Harmonic Distortion (*THD,* dt. Klirrfator) is another measure for errors based on non-linearity. It computes the energy of the harmonics of the sinusoidal signal with frequency f_1 compared to the energy at f_1 or the total signal energy.

$$THD = \frac{P_{Distortion}}{P_{Signal}}, \qquad THD_{dB} = 10dB \cdot \log\left(\frac{\sum_{k=2}^{N} \left|X(f_k)\right|^2}{\left|X(f_1)\right|^2}\right) \quad \text{with} \quad f_k = k \cdot f_1,$$

2.4.7 SINAD

Signal to Noise And Distortion: $SINAD = \dfrac{P_{Signal}}{P_{Noise} + P_{Distortion}}$.

Some sources as https://en.wikipedia.org/wiki/SINAD define $\dfrac{P_{Signal} + P_{Noise} + P_{Distortion}}{P_{Noise} + P_{Distortion}}$.

2.4.8 *ENOB*: Effective Number of Bits:

If an *ADC* offer 16 output pins, but only 12 of them are accurate, the rest is noise, then *ENOB*=12. These supernumerary pins might have several reasons, e.g. inaccuracies in the most significant bits or noise in the input signal of the considered ADC. Offering 16 pins instead of 12 may be reasonable e.g. for pin-compatibility with more expensive *ADCs*.

$$\boldsymbol{ENOB} = \frac{SINAD - 1.76dB}{6.02dB} ,$$

which assumes a sinusoidal test wave and triangular quantization noise waveforms. In case of rectangular quantization noise waveforms replace "-1.76dB" by "+3.01dB".

2.5 Comparison of ADC Architectures

Tab. 2.5.1 illustrates a comparison of the most important properties of the most important ADC architectures according to [1].

ADC Type	**Flash**	**Pipeline**	**SAR**	**ΣΔ**
Throughput	++	++	o	o
Delay	++	-	o	--
Resolution	--	++	+	+++
Suitable for multiplexing	+	+	+	--
Simplified or no anti-aliasing filter	no	no	no	yes
Subsampling possible	yes	yes	yes	no

Tab. 2.5.1: Comparing features of the most important ADC architectures.

Application Example: 16 input channels are to be sampled within a bandwidth of 0...100KHz with a resolution of 14 bits. This corresponds to a total bandwidth of $16 \cdot 100\ \text{KHz} = 1.6\ \text{MHz}$. According to Nyquist, the sampling rate must be at least twice of that, i.e. **3.2 MS/s**. Tab. 2.5.2 compares 3 ADC's with differenc architectures if they are suitable for this task. The table is some years old, nowadays converters may be faster, but tendency is the same.

ADC type	**Architecture**	**Total throughput T at 14 bit resolution in KS/s**	**Effective multiplexed throughput in KS/s: $T_{mux}=1/\tau_{delay}$**	**Number of ADCs required**
AD7865	SAR	416	416	8
AD7722	ΔΣ	220	2.3	1392
AD9240	Pipeline	10 000	10 000	1

Tab. 2.5.2: Comparison of different ADC topologies for a particular multiplexing task.

2.6 References

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