**ESS Section 3**

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**Procedure.** In class, this MS Word document is written using a tablet PC. Page breaks and/or subsection headings can be moved. After class, students are offered both the modified Word document and a PDF printout of it.

# A/D and D/A Converter Modeling

## D/A Converter (DAC) Modeling

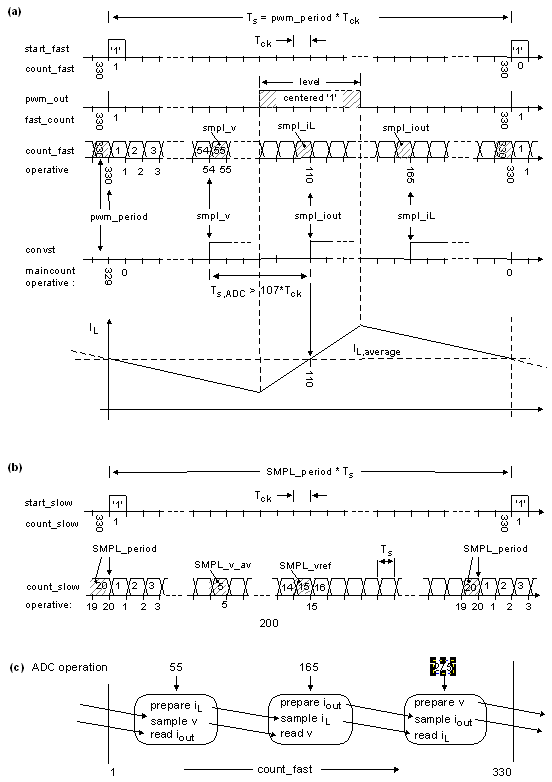
### Conventional D/A Converter

### Switch-Mode D/A Converter

## A/D Converter (ADC) Modeling

## Miscellaneous

### PWM DAC and ADC-Sampling Used for *DCDCbuck Rev*.10 and 11



**Fig. 3.3.1:** Timing diagram with starting-'1' output, *Tck* = 1 / *fck* = 1/ 50MHz. Sampling coil durrent *IL* in the middle of the High- or Low-phase delivers its average value in CCM.

### Handling A/D and D/A Conversion within a Loop

### Need for Synchronous Sampling

### Limit Cycling

### Describing Function

## References

1. *Linear Technology (today: Analog Devices)*, “*Low Noise, 500ksps,  
   8-Channel, 12-Bit ADC*”, available: https://www.analog.com/media/en/technical-documentation/data-sheets/2308fc.pdf